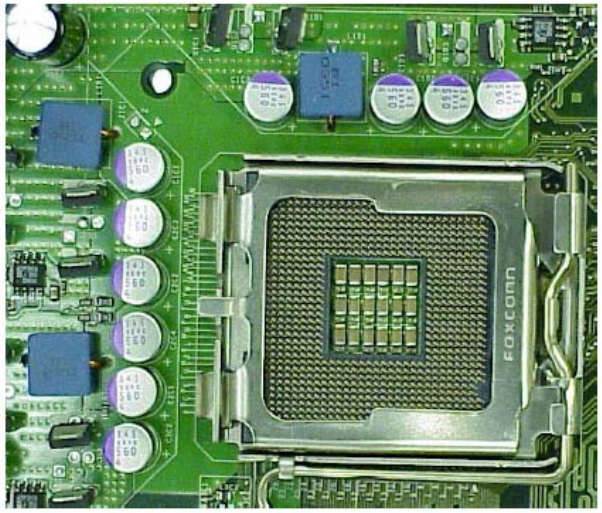
Power Integrity
and
Decoupling of **Fast** Integrated Circuits

AFCEM

RF & Microwave



Yves Leduc,
Associate Member, Polytech'Lab,
University of Nice Sophia-Antipolis
Sophia-Antipolis

Nathalie Messina,
Multimedia Function Architect & Feature Reference,
Magneti Marelli Infotainment & Telematics,
Sophia-Antipolis

Power Supply Impact on IC's Functionality

How the power is supplied to an integrated circuit greatly affects the functionality of the system:

- ***External bypass capacitors cannot address the high frequencies issues [e.g. Fujitsu_02].***

Not enough anymore…

Supplying power to high speed integrated circuits is a challenging task:

- ***L di/dt must complement iR Static and Dynamic Drop analysis ☠.***

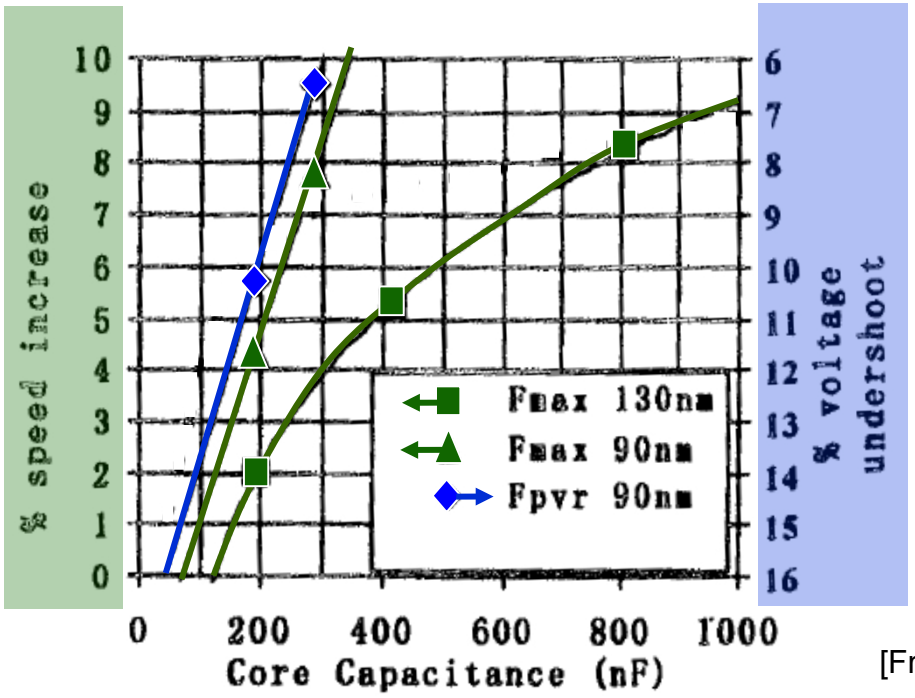
Fast I transient

High average I

Power Supply Impact on IC's Performances

How the power is supplied to an integrated circuit may affects the performances of the system:

- ***Power Supply noise limits the maximum operating frequency of an integrated circuit*** *[PDN_04, Free_06, …]*



[Free_06]

Freescale gains
8% of performances
by on chip bypassing

NB: *C035 130nm*
C027 90nm

Definitions

Decoupling

- ***The art and practice of breaking coupling between portions of systems and circuits to ensure proper operation.***

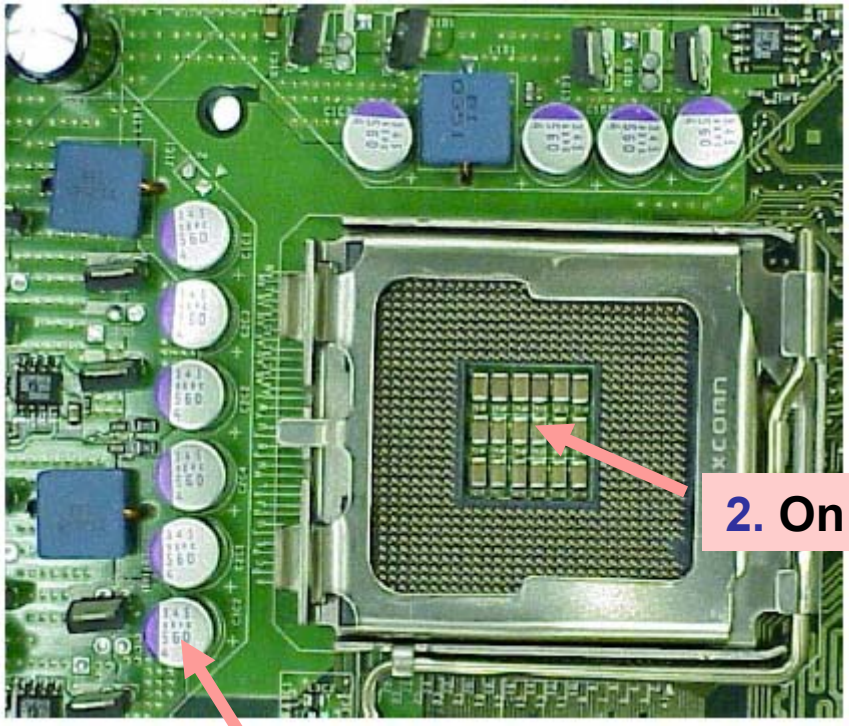
Bypassing

- ***The practice of adding a low-impedance path to shunt transient energy to ground at the source. Required for proper decoupling.***

[Cypress Semiconductor Corporation 1999]

Bypassing Strategy, an Example: the **Pentium 4™**

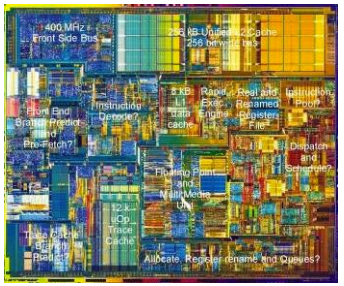
4 levels of Bypassing



2. On PCB (Socket)

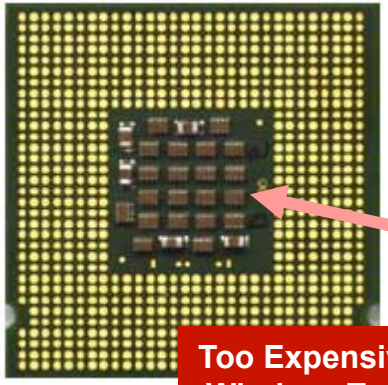
1. On PCB (Source)

4. On Chip



top view

bottom view



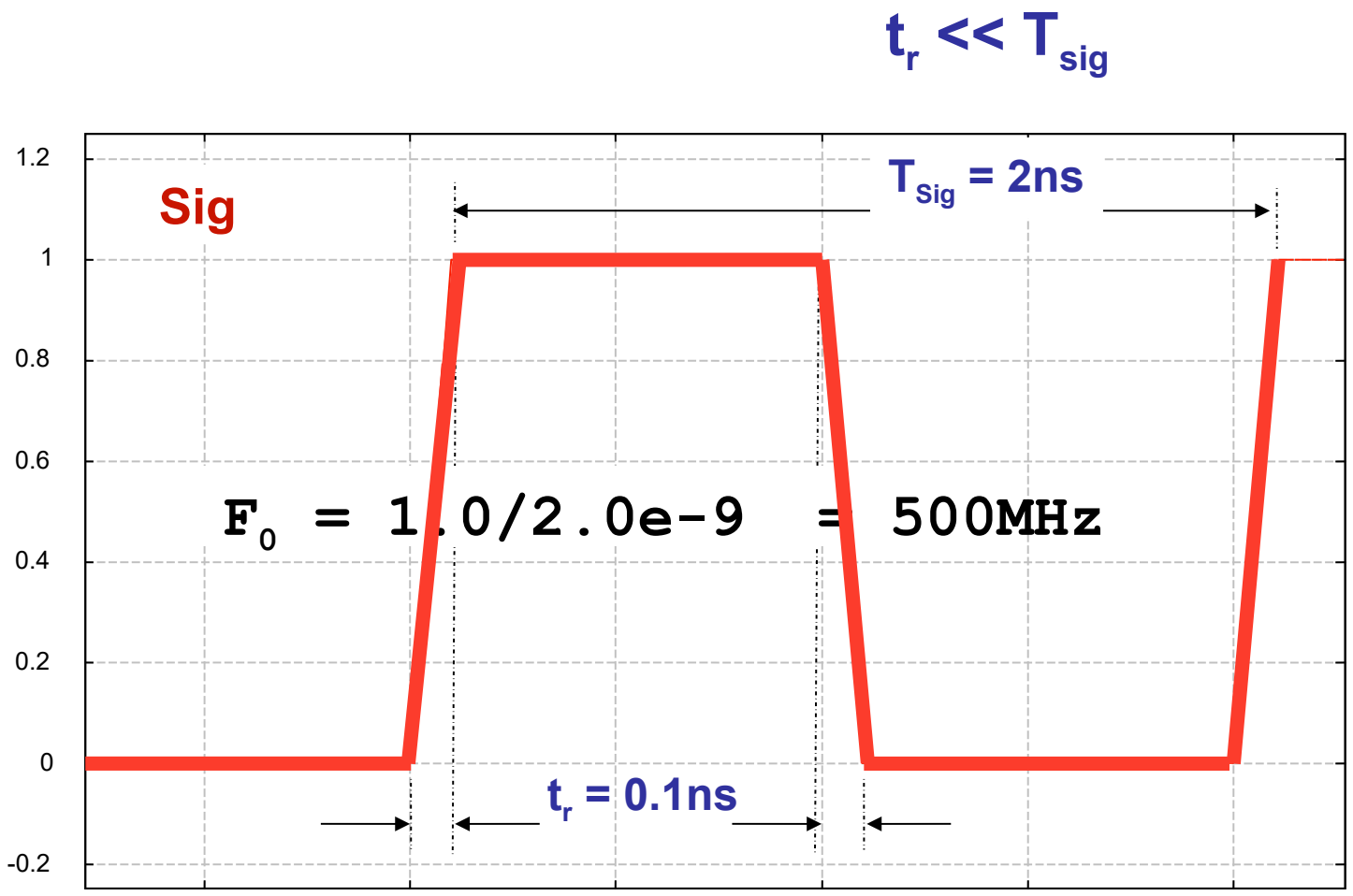
3. In Package

Too Expensive in a Wireless Terminal

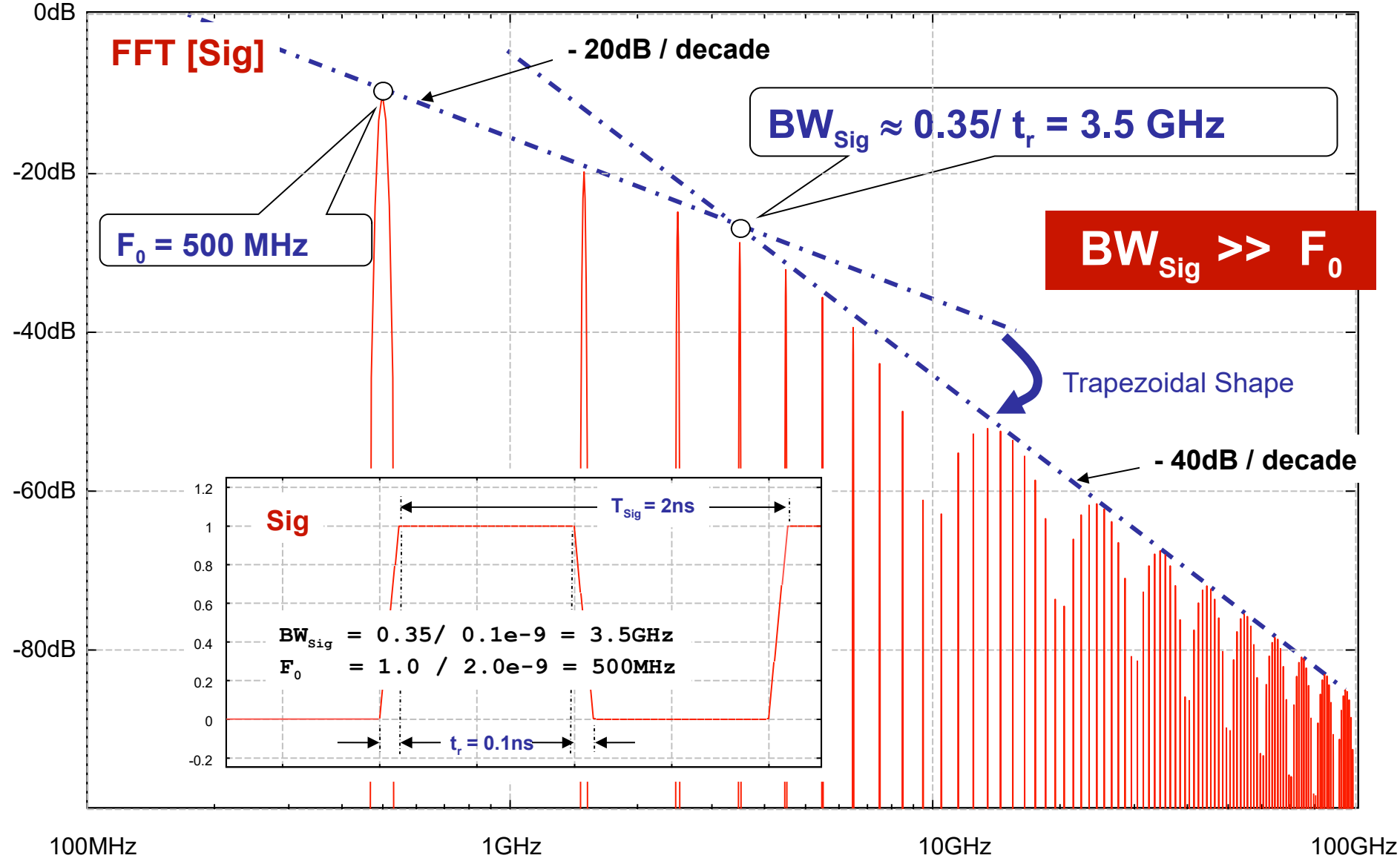
AGENDA

1- **Bandwidth of Interest**
2- Model of a Power Distribution System
3- Bypassing Examples
4- Bypassing Methods
5- IC and PCB Designers Point of View
6- Power Distribution System Model Extraction
7- Conclusion

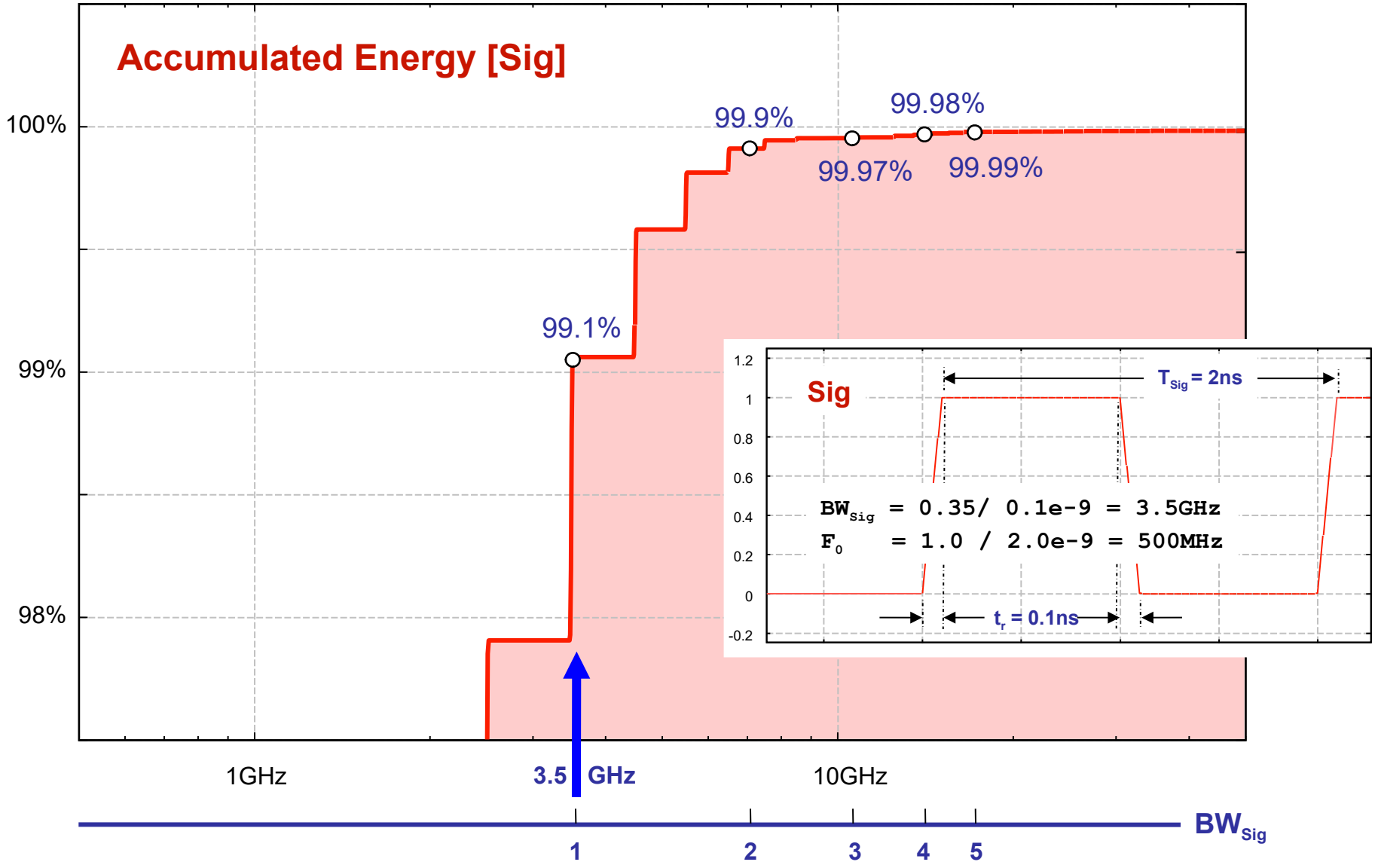
A Trapezoidal On-Chip Signal



Bandwidth of a Trapezoidal Signal



Energy in a Trapezoidal Signal

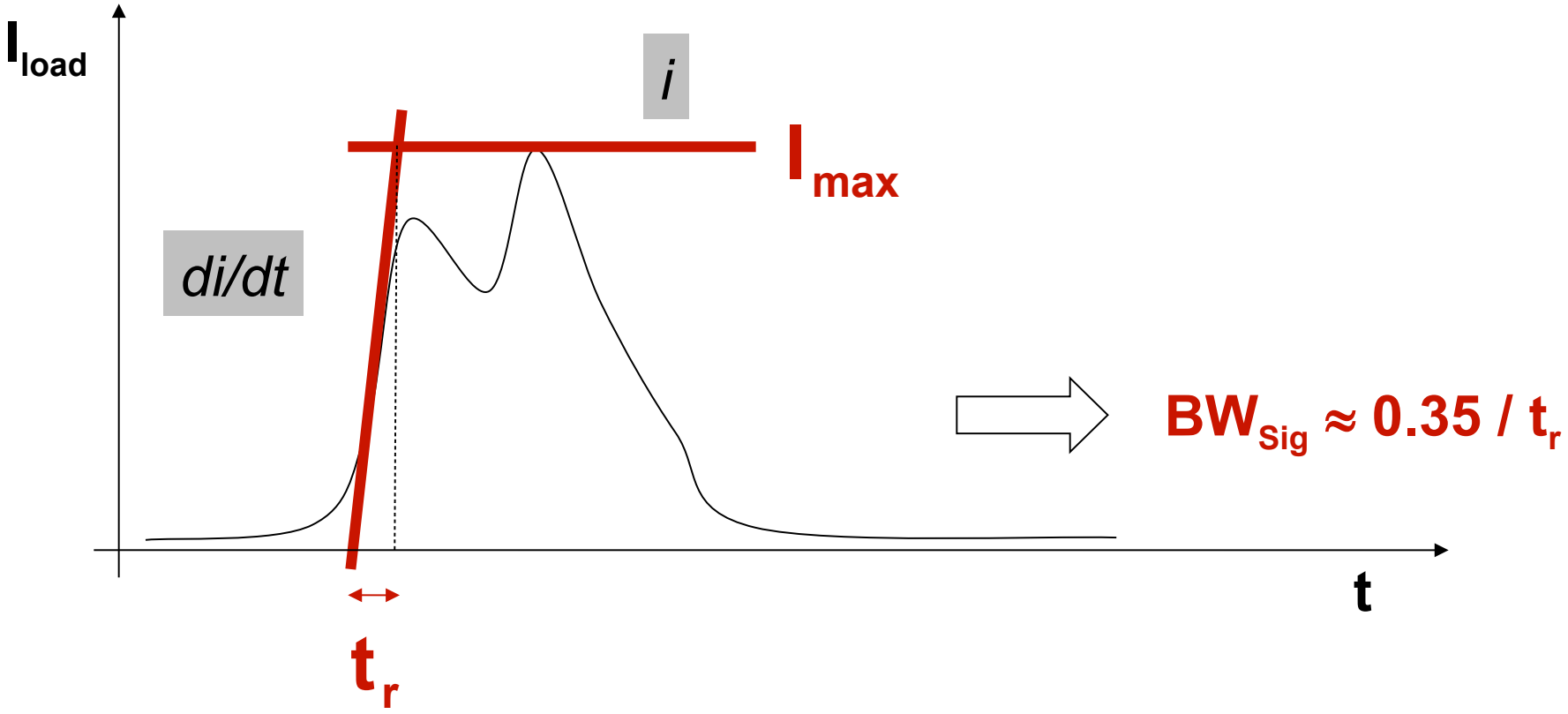


AGENDA

1- Bandwidth of Interest
2- **Model of a Power Distribution System**
3- Bypassing Examples
4 Bypassing Methods
5- IC and PCB Designers Point of View
6- Power Distribution System Model Extraction
7- Conclusion

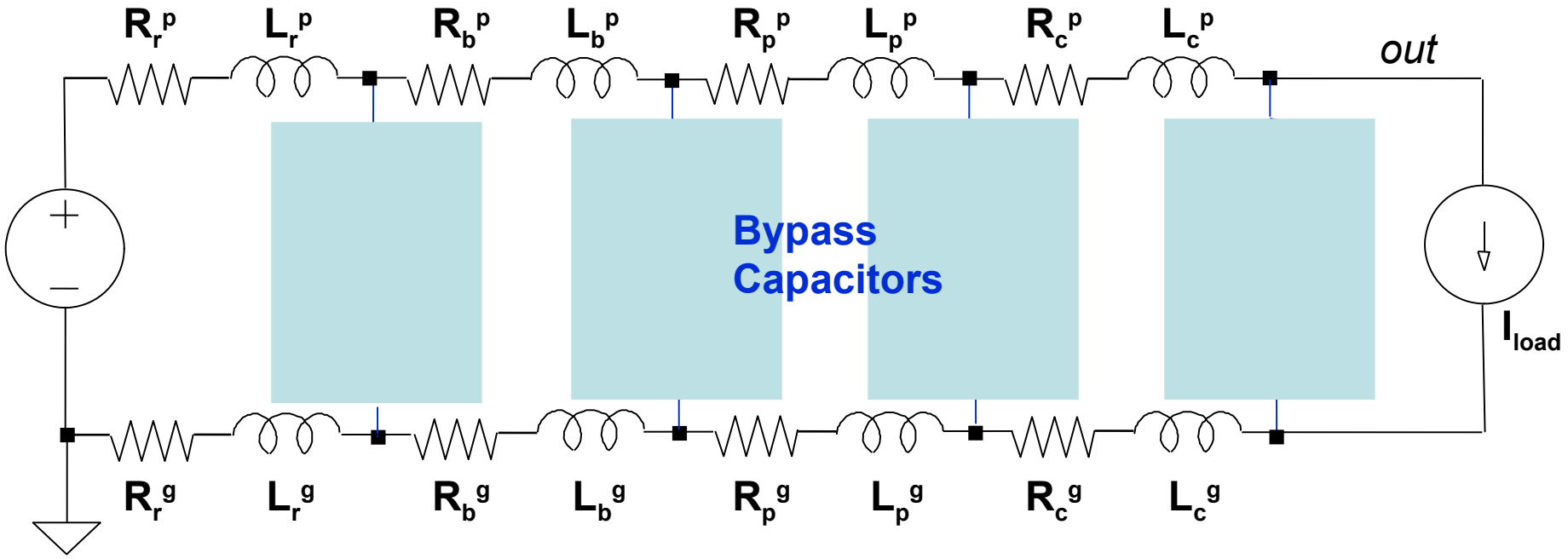
Modeling with a Trapezoidal Simplified Model

In a **Power Distribution System**, the signal is a **Current Surge**.



Simplified Model of a Power Distribution System: RLC

NB: Global ground does not exist!



The power source and the load are connected through resistive and **inductive** parasitic impedances.

Power Distribution System Target Impedance

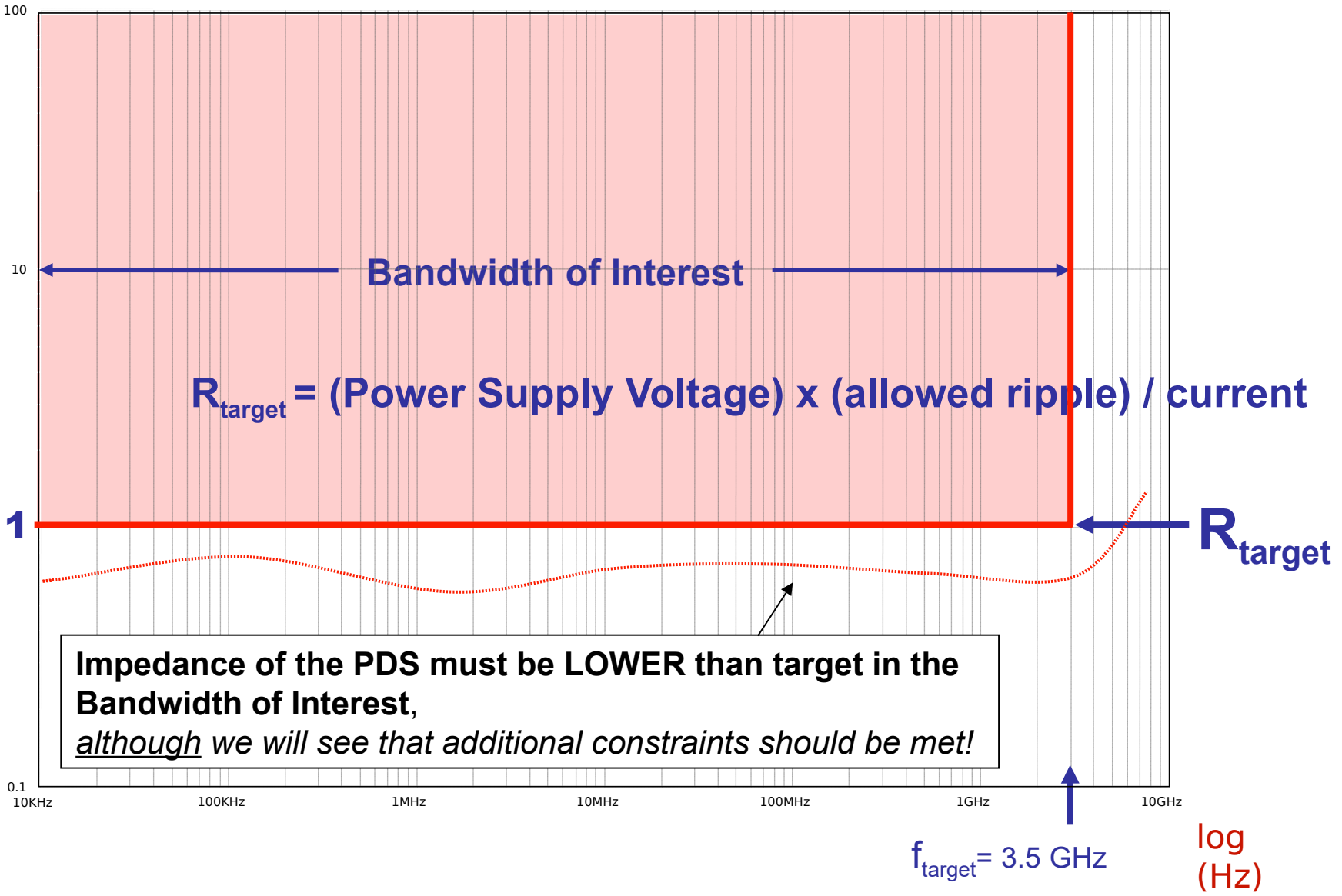
V_{dd} = Power Supply Voltage [V]
Tol = Allowed Ripple [%]
I_{max} = Max Load Current [A]

$$\mathbf{R_{target} = V_{dd} \times (Tol /100) / I_{max}}$$

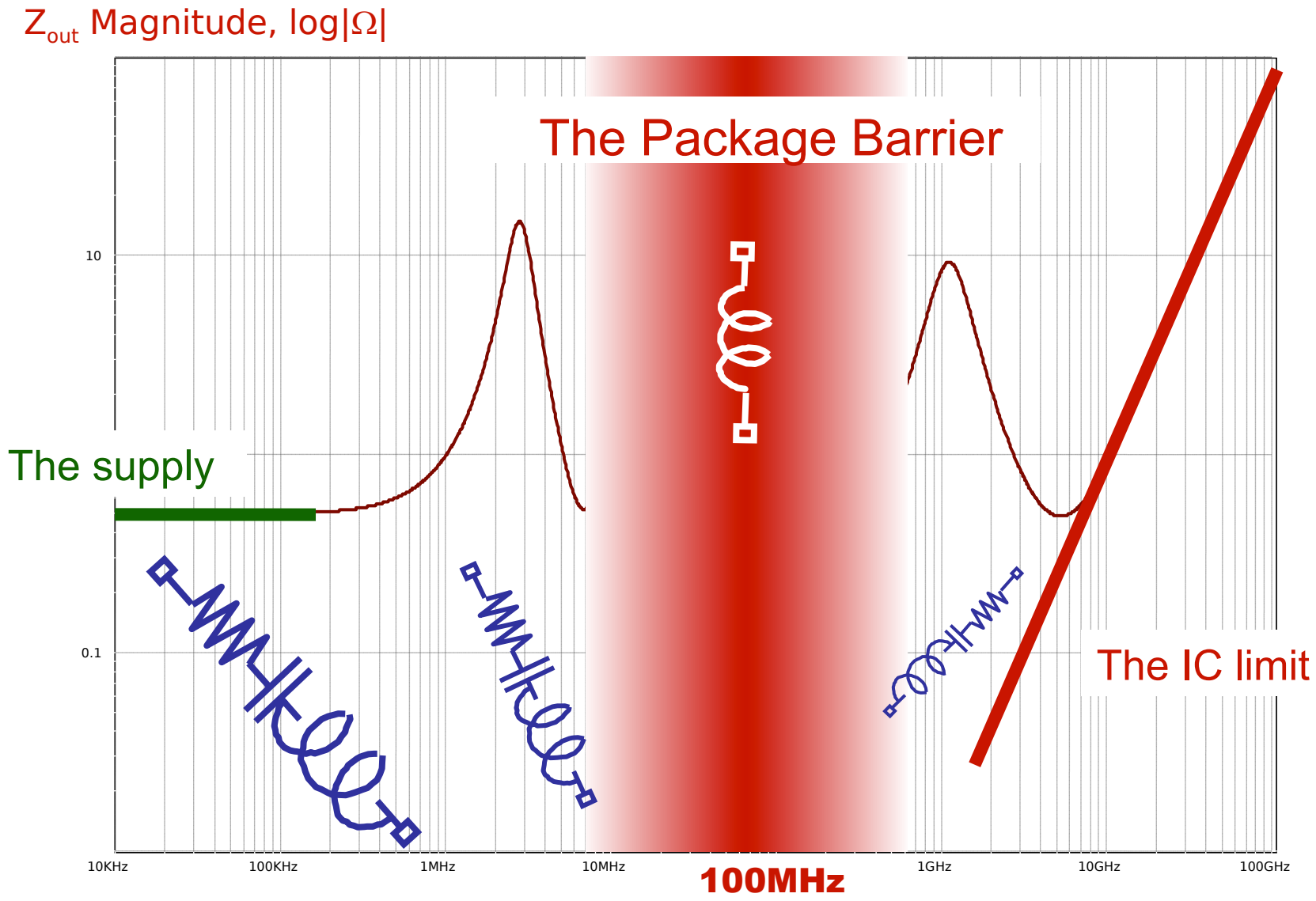
For example,

with an allowed ripple of 10% on a Vdd of 1V
and a max load current of 100mA,
the target impedance will be 1Ω

Power Distribution System Target Impedance



PCB Bypassing does not Solve IC Issues



AGENDA

1- Bandwidth of Interest
2- Model of a Power Distribution System
3- **Bypassing Examples**
4- Bypassing Methods
5- IC and PCB Designers Point of View
6- Power Distribution System Model Extraction
7- Conclusion

FYI, Some Orders of Magnitude

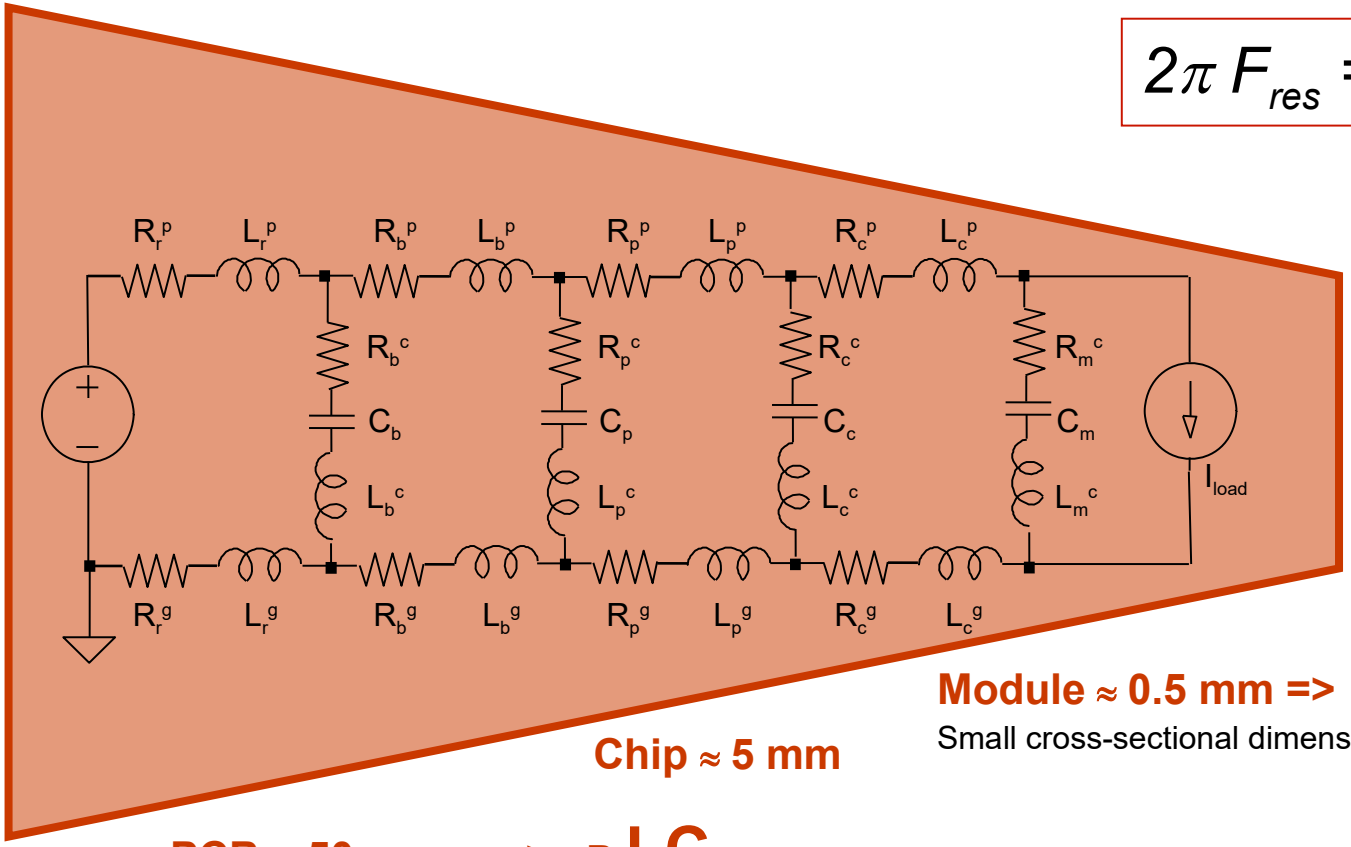
Package 424ZQX	***0.3nH … 5nH***
	15mΩ …180mΩ
	0.1pF … 0.6pF
Bond Wire	***50mΩ /mm***
	1nH /mm
	0.05pF /mm
Typical PCB Line	***0.5nH /mm***
	0.1pF /mm
	5mΩ /mm
Via through 1.6mm PCB	***1.3nH***
0402 Capacitor	*100nF*
	0.5nH
	25mΩ

Rule of Thumb

L ≈ 1nH /mm

Linear Variation of L and R with the Circuit Dimensions

$$2\pi F_{res} = 1 / \sqrt{LC}$$



Chip ≈ 5 mm

Module ≈ 0.5 mm => R LC

Small cross-sectional dimensions of the IC interconnect

PCB ≈ 50 mm => R LC

Large cross-sectional dimensions of PCB interconnect

Physical dimensions ➡

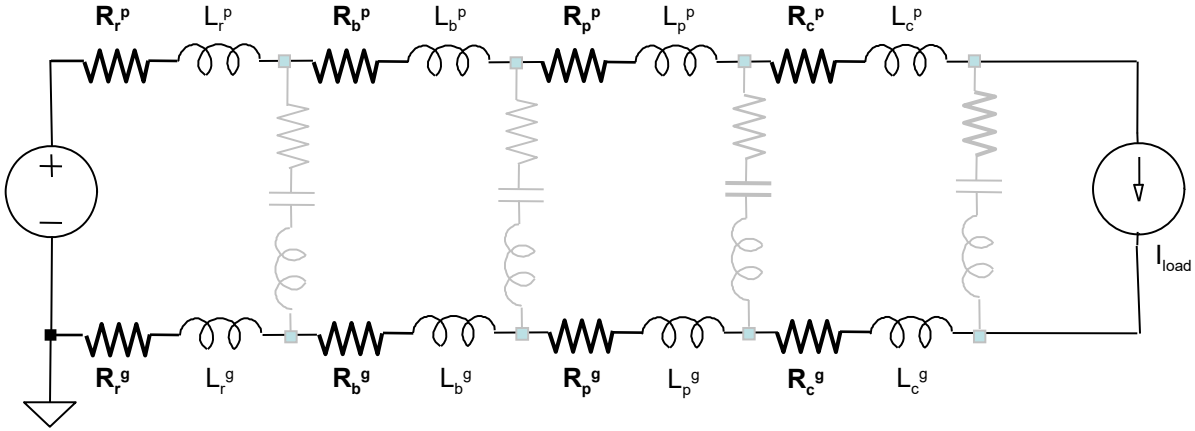
$$L_r >> L_b >> L_p >> L_c$$
$$R_r << R_b << R_p << R_c$$
$$C_b >> C_p >> C_c >> C_m$$

Our Example

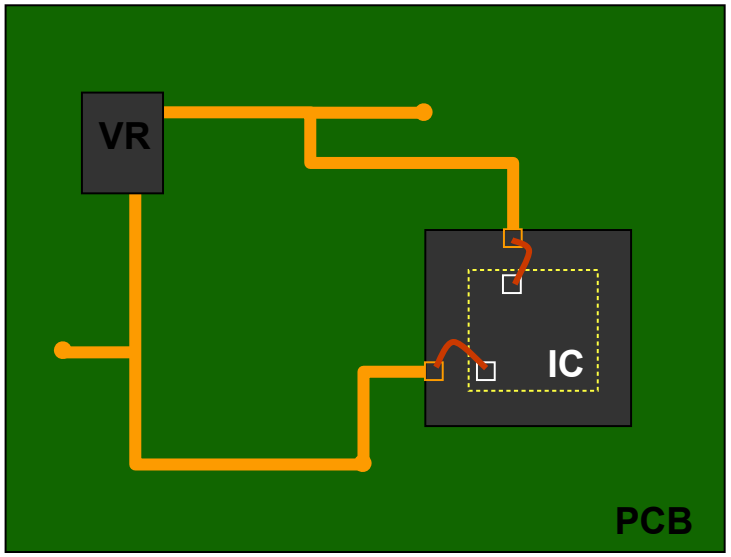
```
******  TARGET

.PARMS Z0 1.00
```

```
******  PDN BOARD

.PARMS Rr 0.25
.PARMS Lr 50.0nH

.PARMS Rb 0.10
.PARMS Lb 10.00nH
```

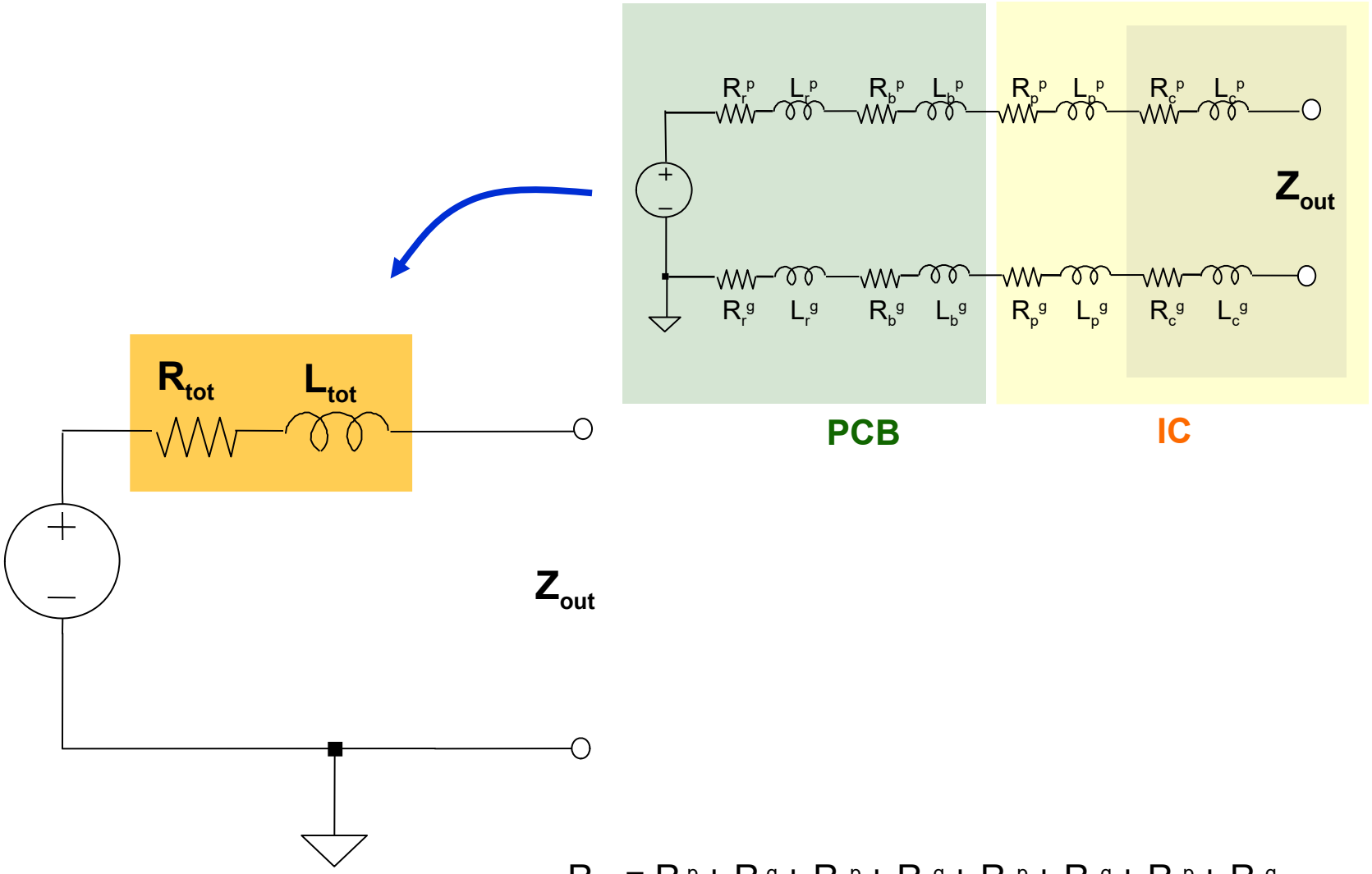
```
******  PDN IC

.PARMS Rp 0.05
.PARMS Lp 1.00nH

.PARMS Rc 0.10
.PARMS Lc 0.10nH
```



VR	PCB	Package	IC



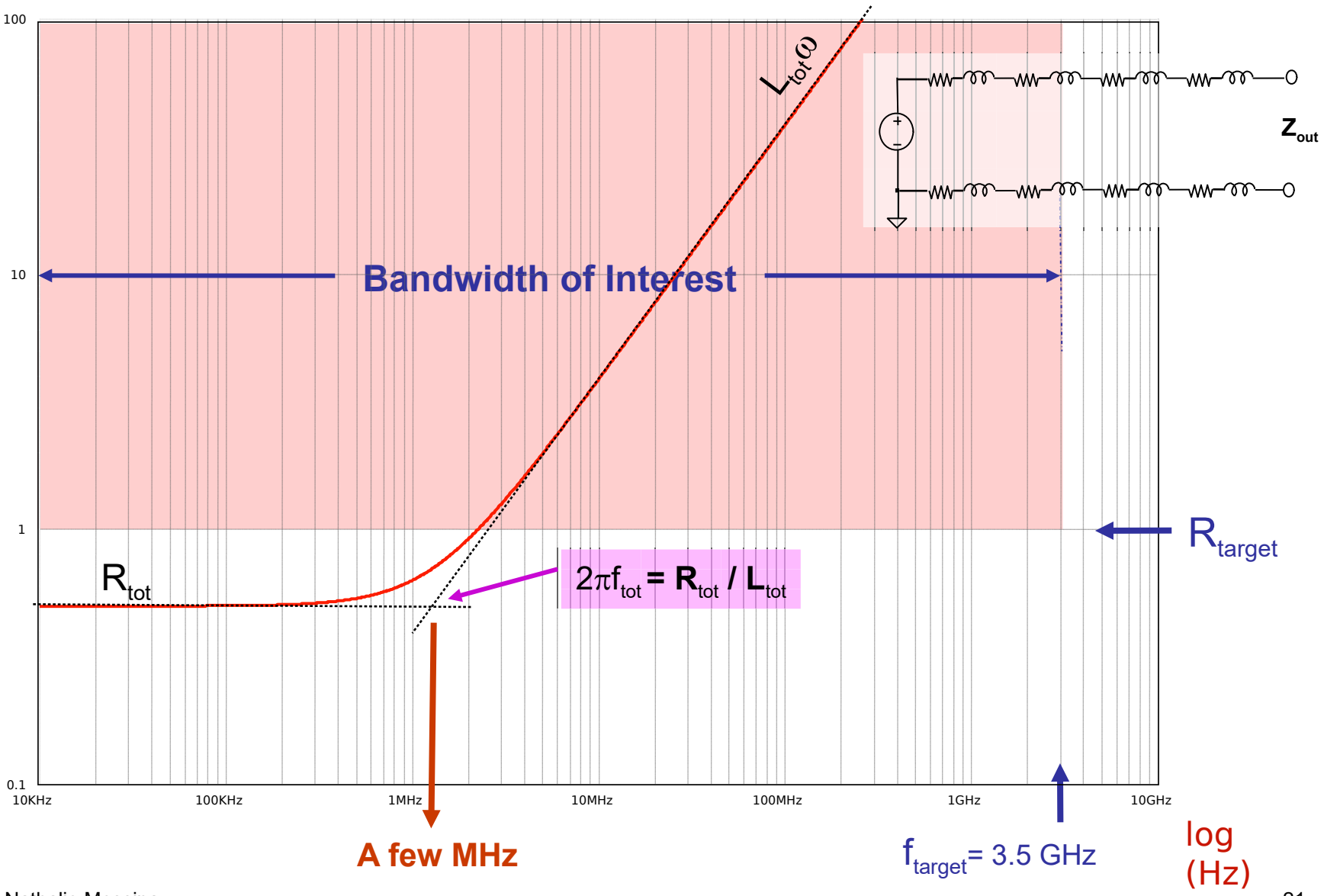
PDS with No Bypass Capacitor



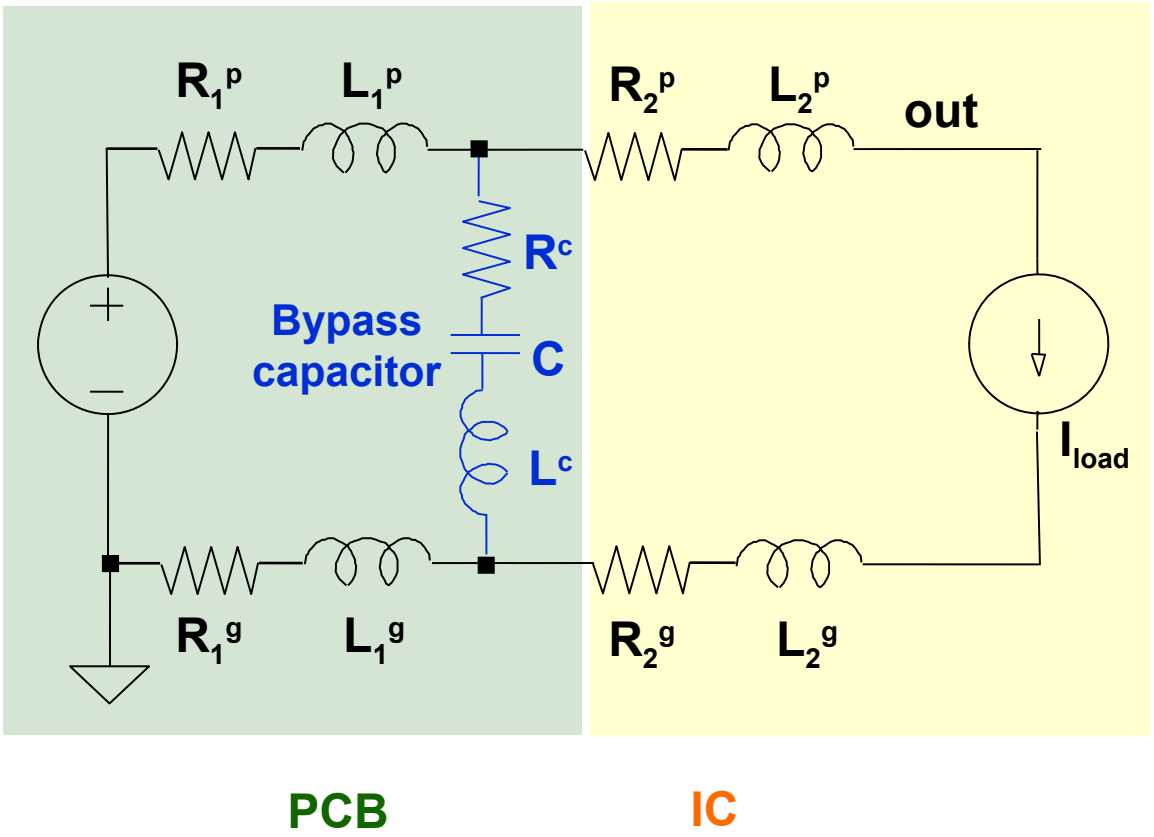
$$R_{tot} = R_r^p + R_r^g + R_b^p + R_b^g + R_p^p + R_p^g + R_c^p + R_c^g$$

$$L_{tot} = L_r^p + L_r^g + L_b^p + L_b^g + L_p^p + L_p^g + L_c^p + L_c^g$$

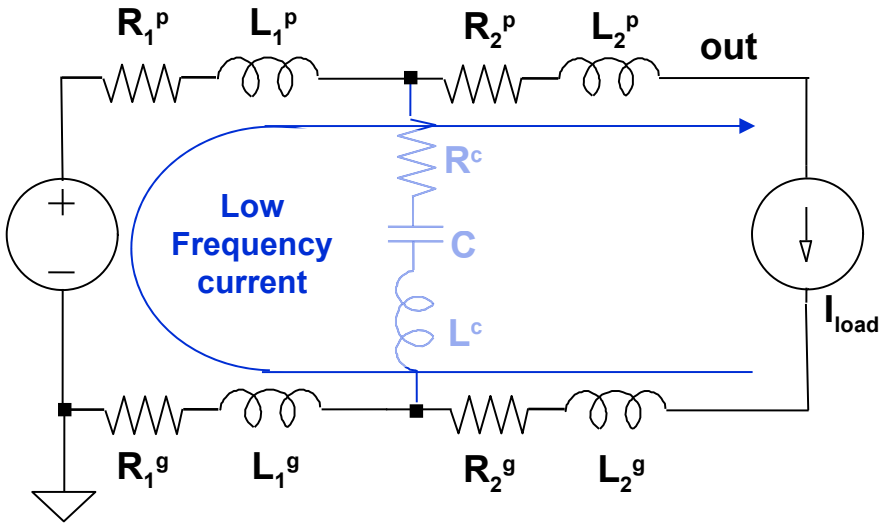
Impedance of a PDS with **No** Bypass Capacitor



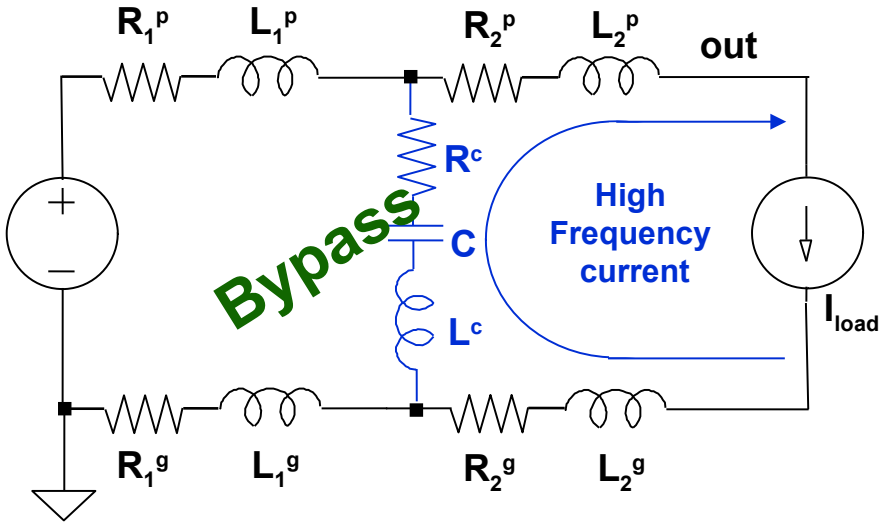
PDS with a Single Bypass Capacitor on PCB



PDS with a Single Bypass Capacitor



Below f_{res}, the bypass capacitance is relatively high.

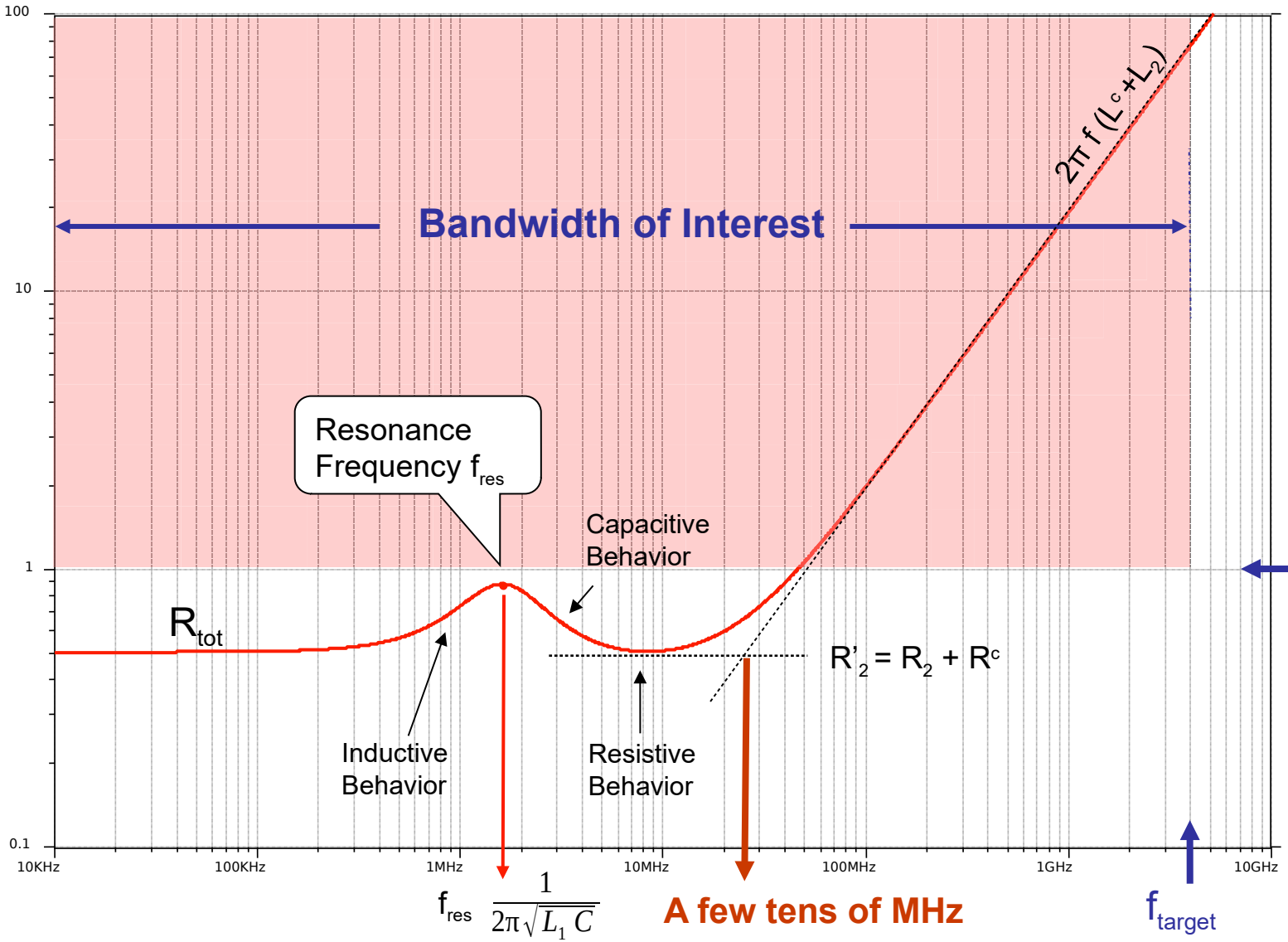


Assuming $L^c < L_1$,

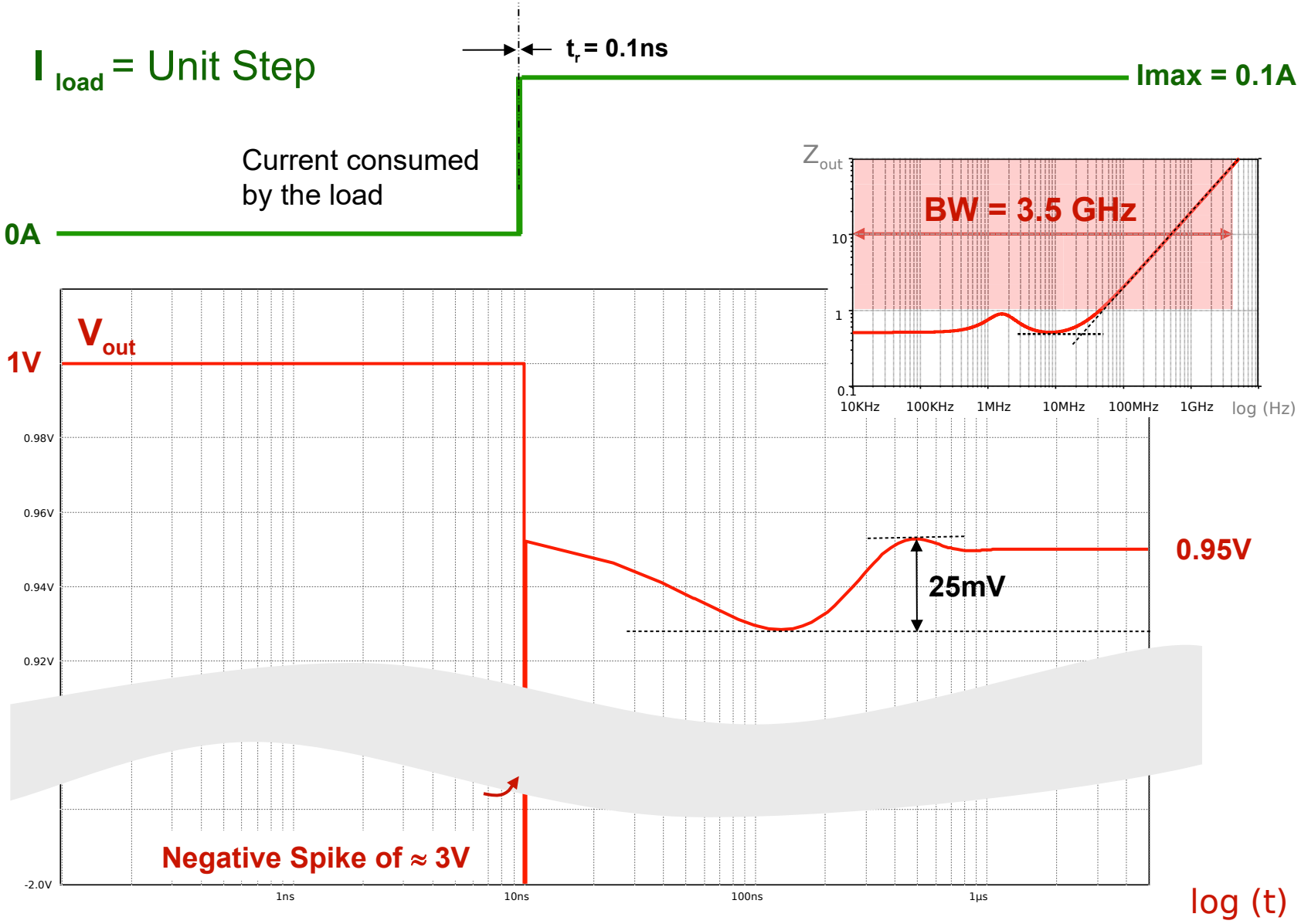
Above f_{res}, the bypass capacitance is lower than the (R1, L1) path.

Impedance of a PDS with a Single Bypass Capacitor

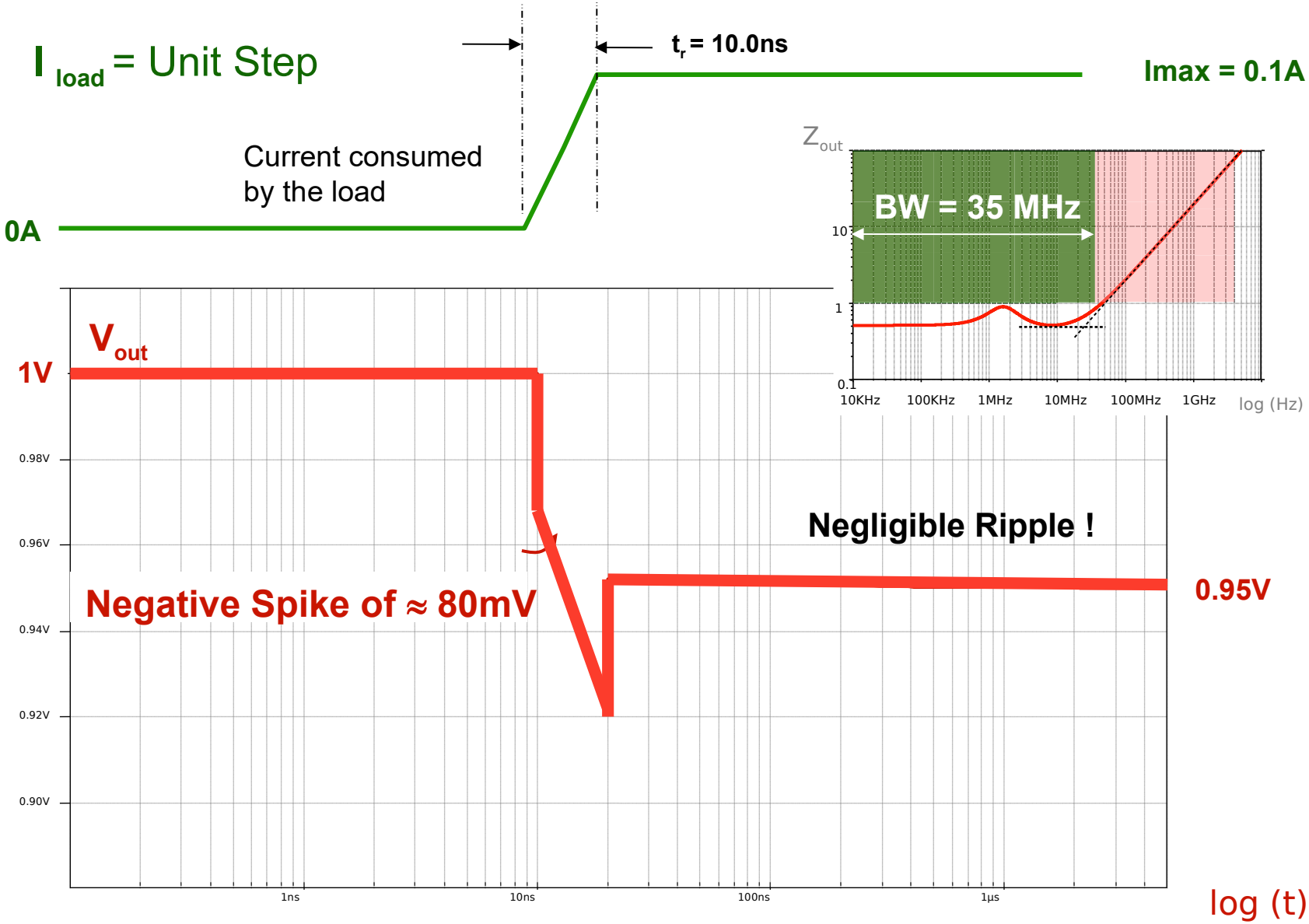
Z_{out} Magnitude, log|Ω|



Transient of a PDS with a **Single** Bypass Capacitor



Just Curious: Let's Increase t_r to 10ns



Limitation from a Single Bypass Capacitor

- The device should have a high capacity to **store and release** a sufficient **amount** of energy

$$C > L_1 / Z_{target}(R_1+R^c)$$

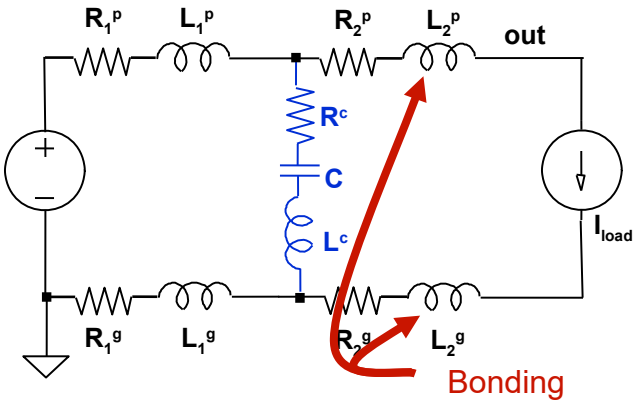
- To supply sufficient power at high frequencies, the device should be able to **store and release** energy at a sufficient **delivery rate**.

$$(L_2 + L^c) < Z_{target} / 2\pi f_{target}$$

The condition of low inductance path cannot be satisfied. Inductance L_2 is the issue:

L_2 ≈ 1 nH
f_{target} ≈ 3 GHz
Z_{target} ≈ 1 Ω

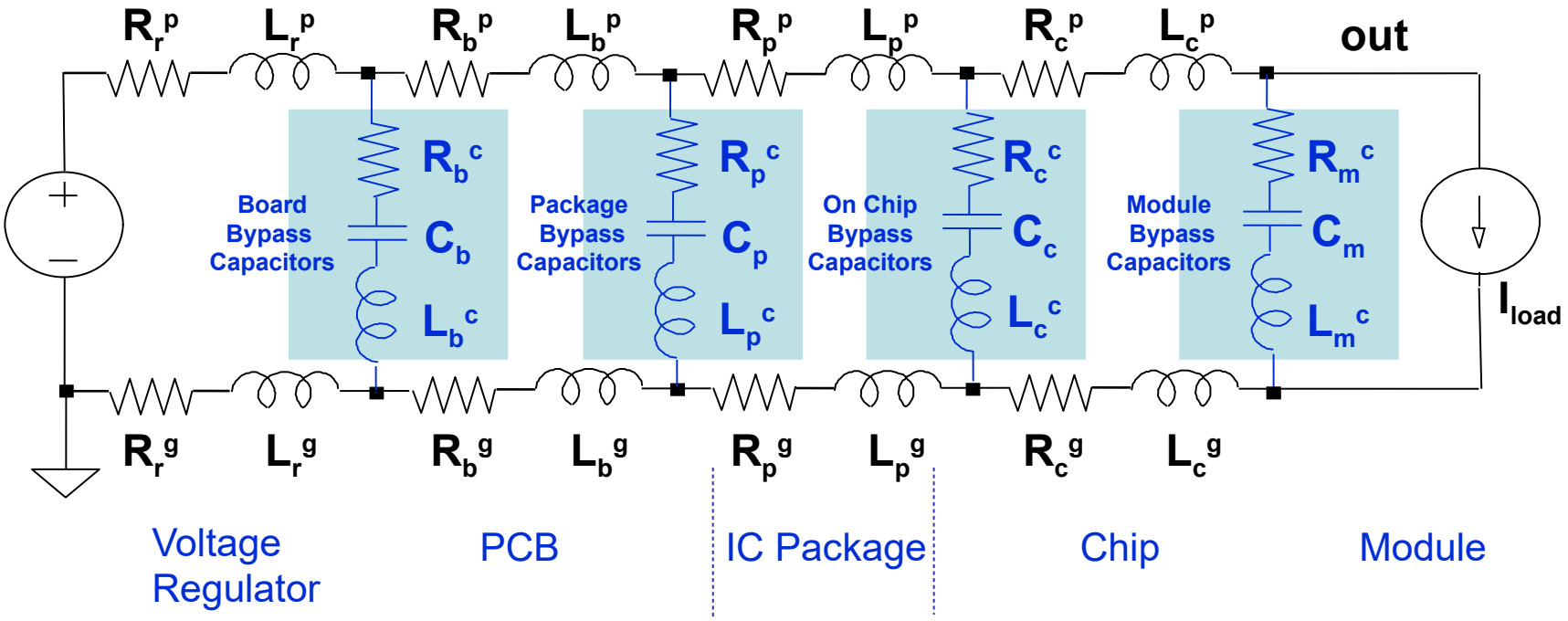
$(1e\text{-}9 + L^c) >> 1 / (6.28 \times 3e9)$



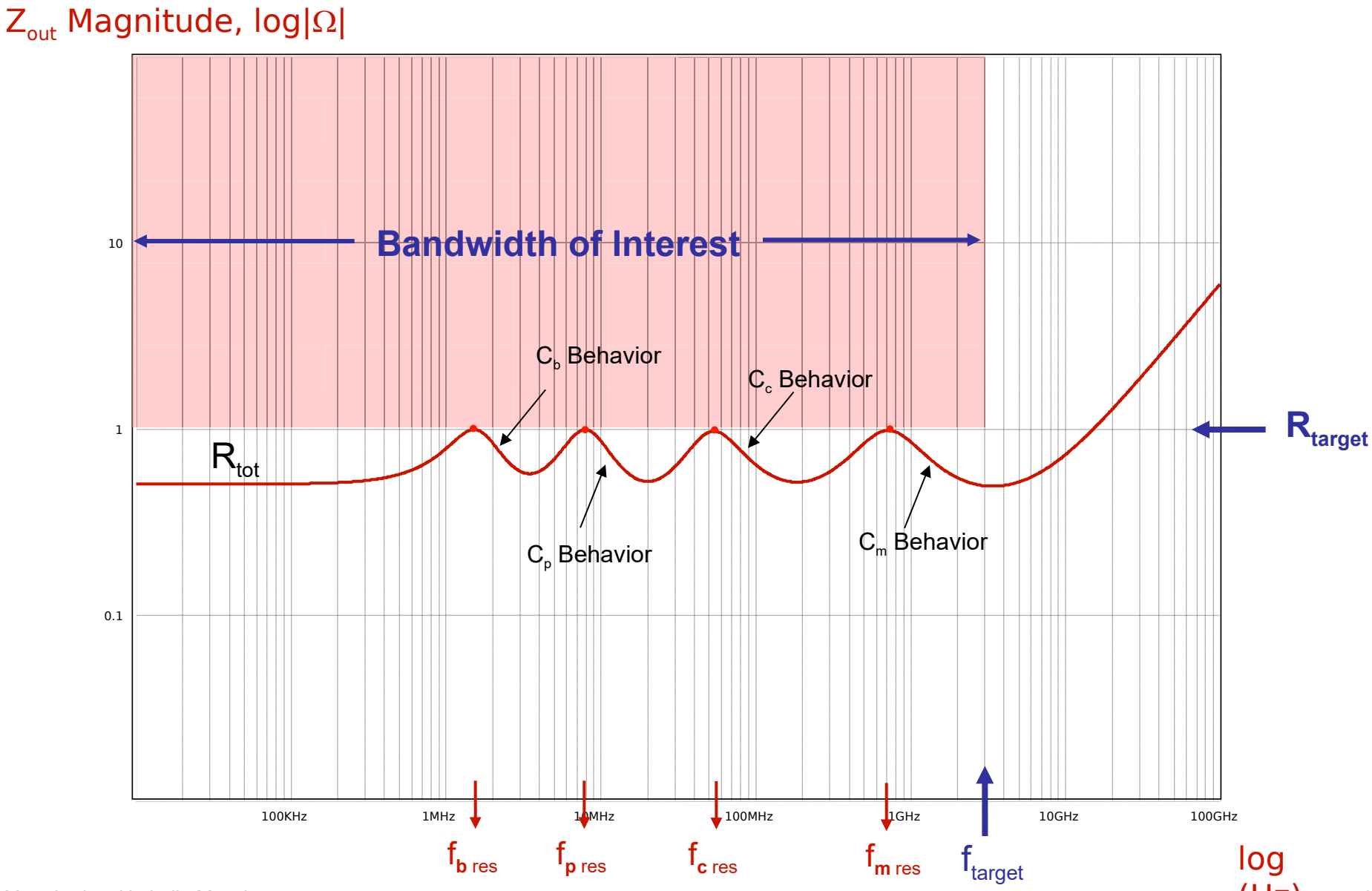
Hierarchical Placement of Bypass Capacitors

Exploits the tradeoff between the capacitance and the parasitic series inductance of a bypass capacitor.

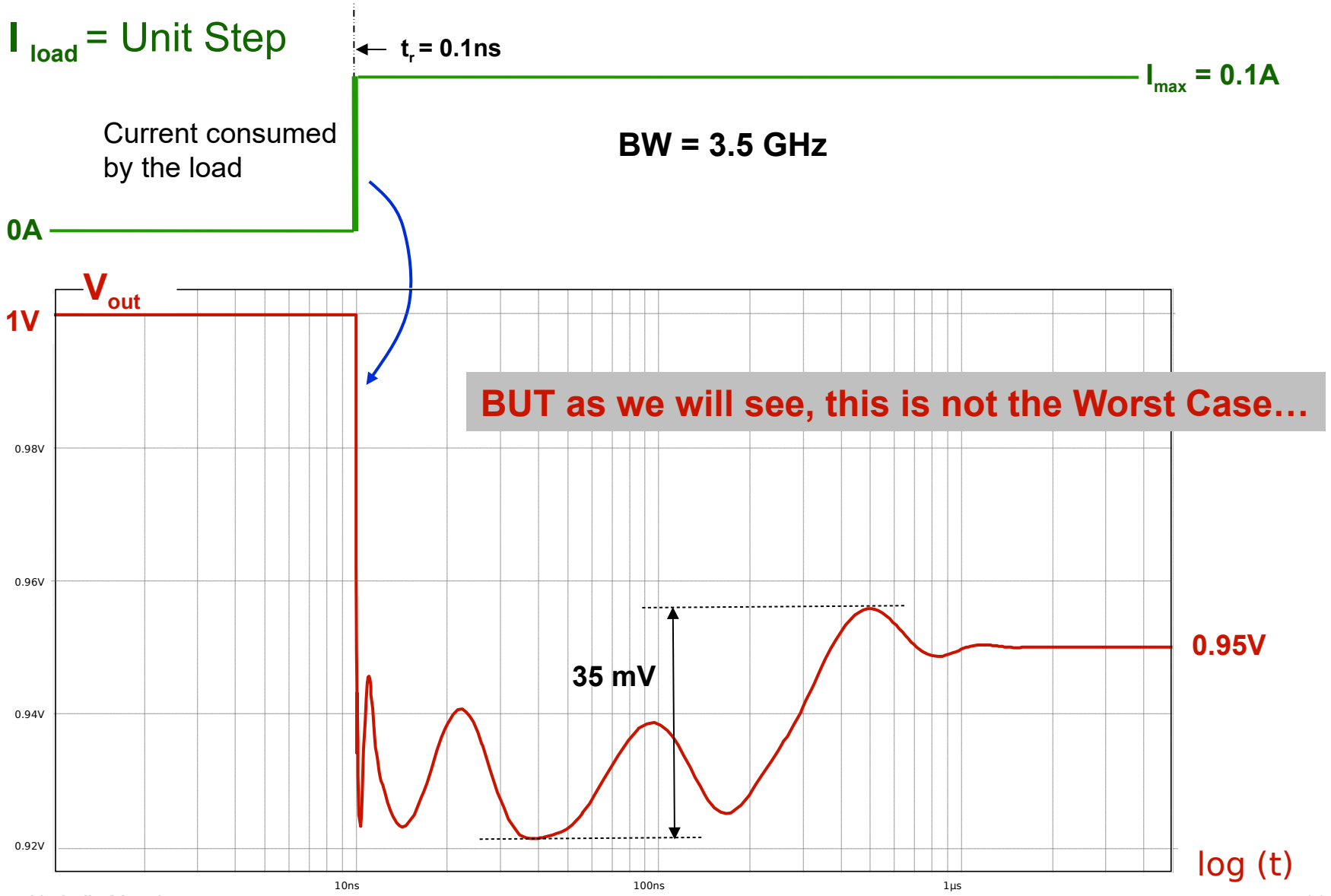
The bypass capacitor at each stage is effective within a limited frequency range. The ranges of effectiveness overlap each other, reaching f_{target}.



Impedance of a PDS with Hierarchical Bypass Capacitors

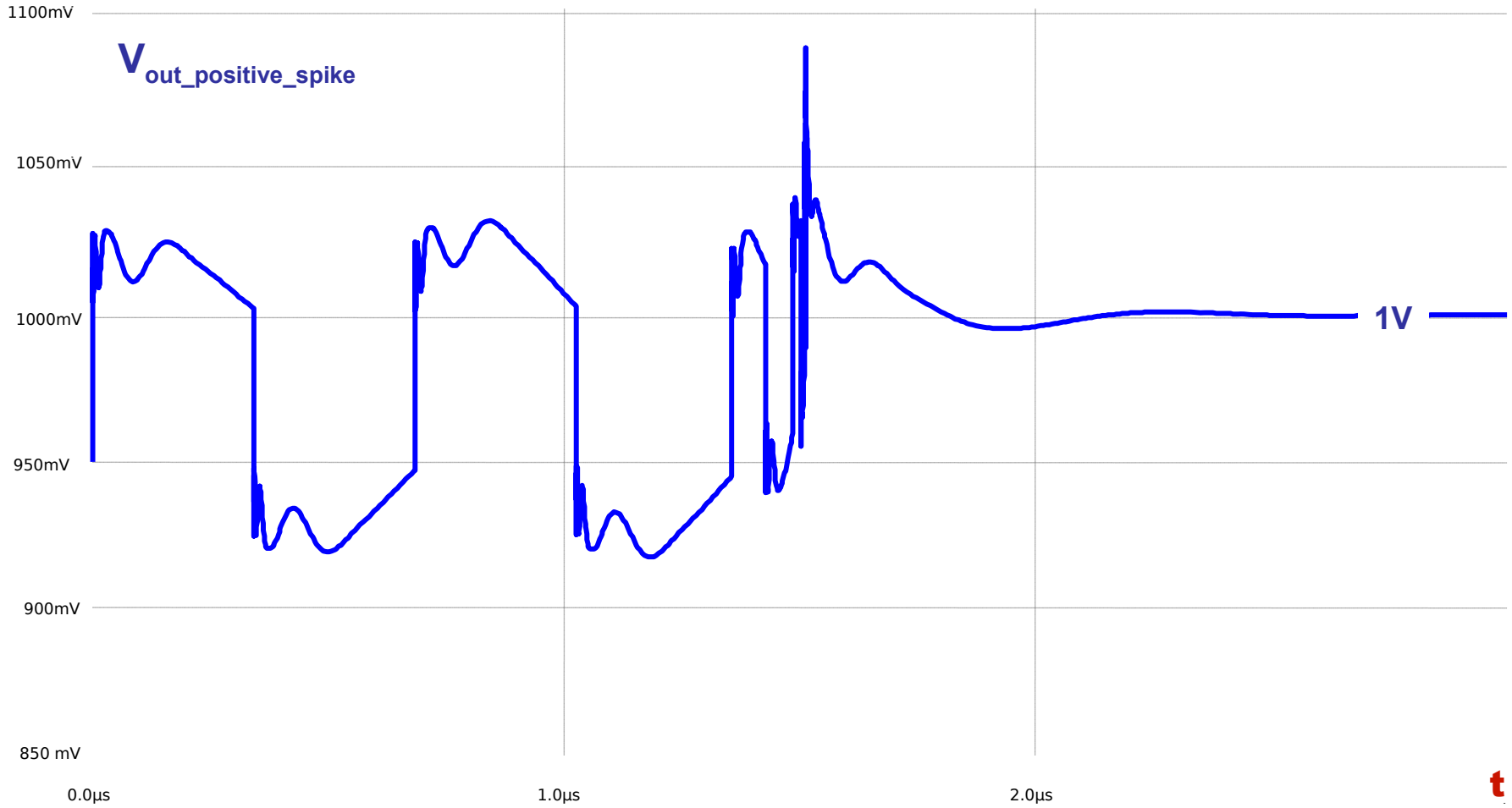


Transient of a PDS with Hierarchical Bypass Capacitors



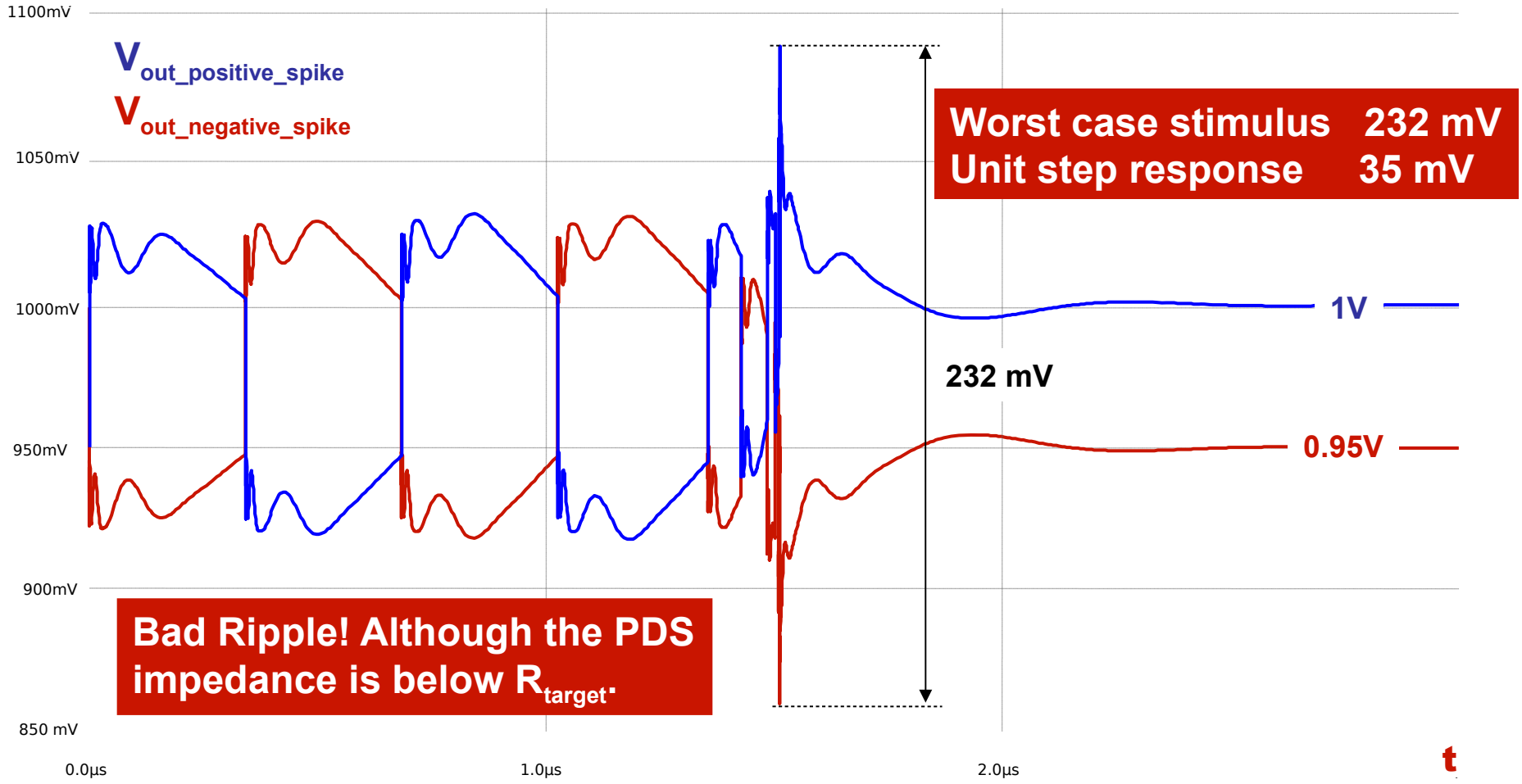
Worst Case Peak Transient

To get the worse case of spikes on the supply voltage, we apply an "**appropriate**" stimulus as I_{load}.

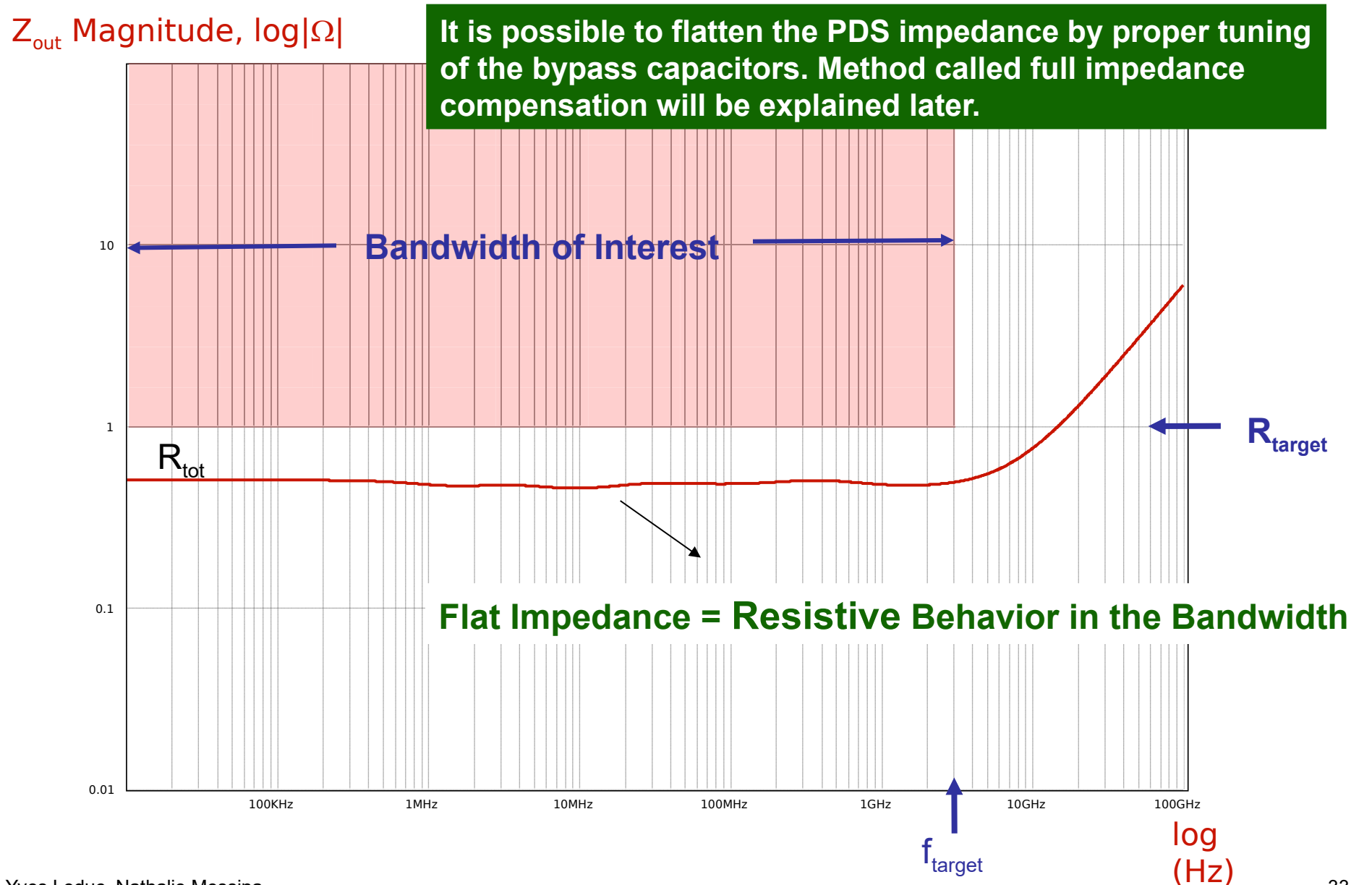


Worst Case Peak-to-Peak Transient

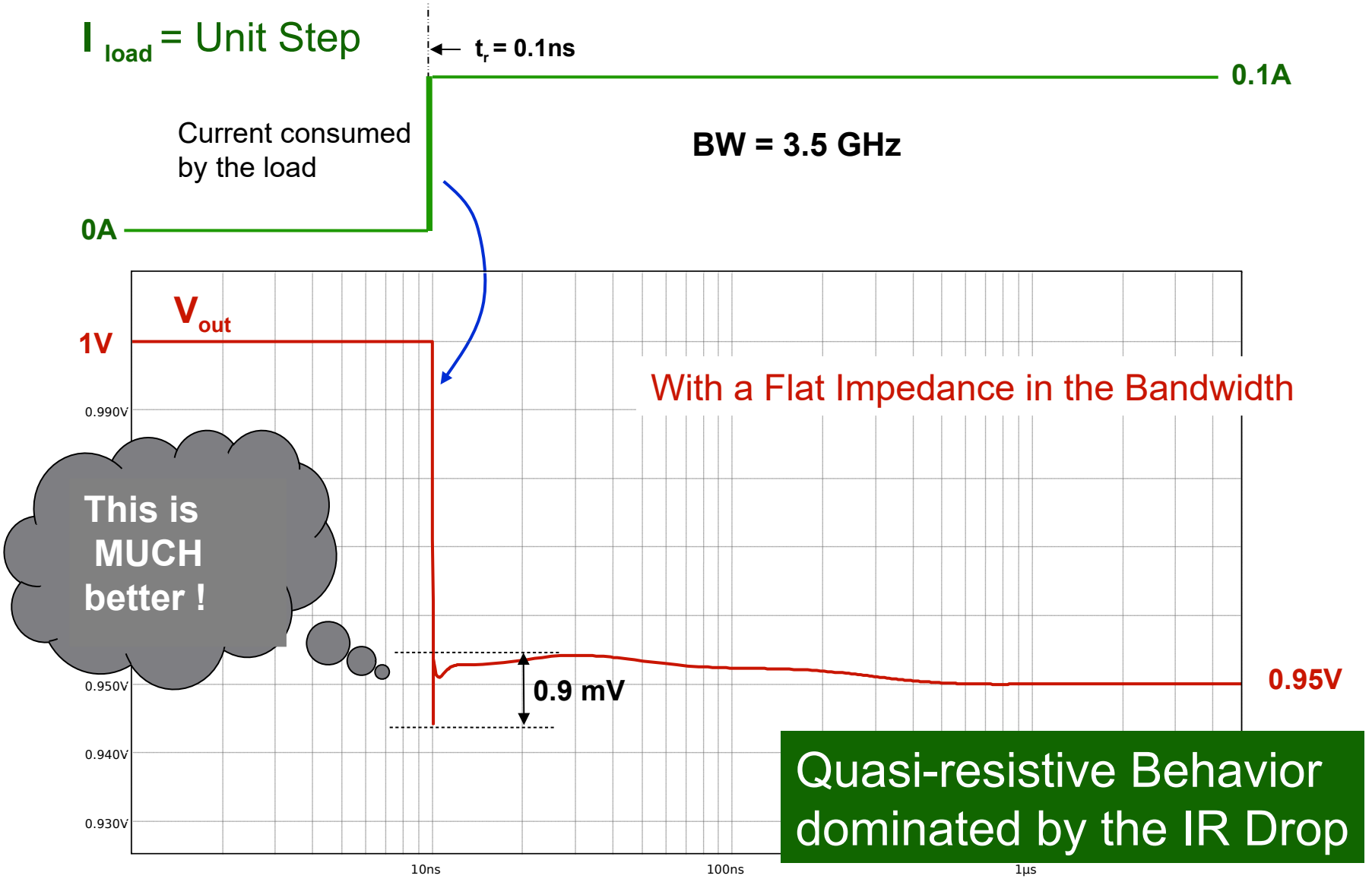
We apply the negative and positive stimulus to get the peak to peak value.



Flat Impedance of a PDS with Hierarchical Bypass Caps



Transient of a PDS with a Flat Impedance

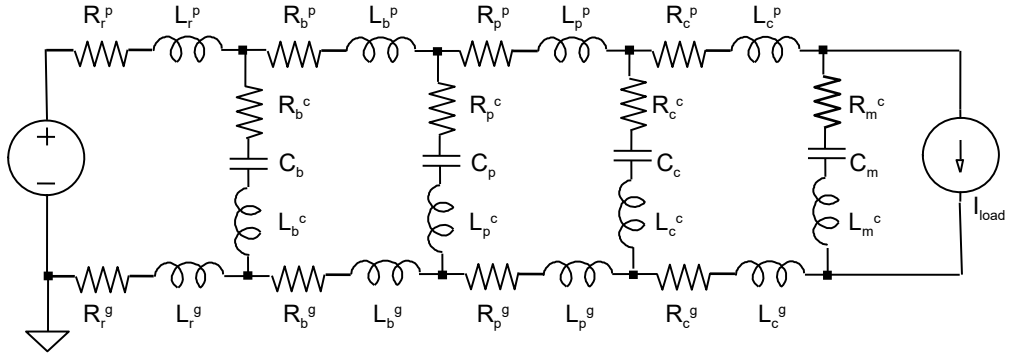


AGENDA

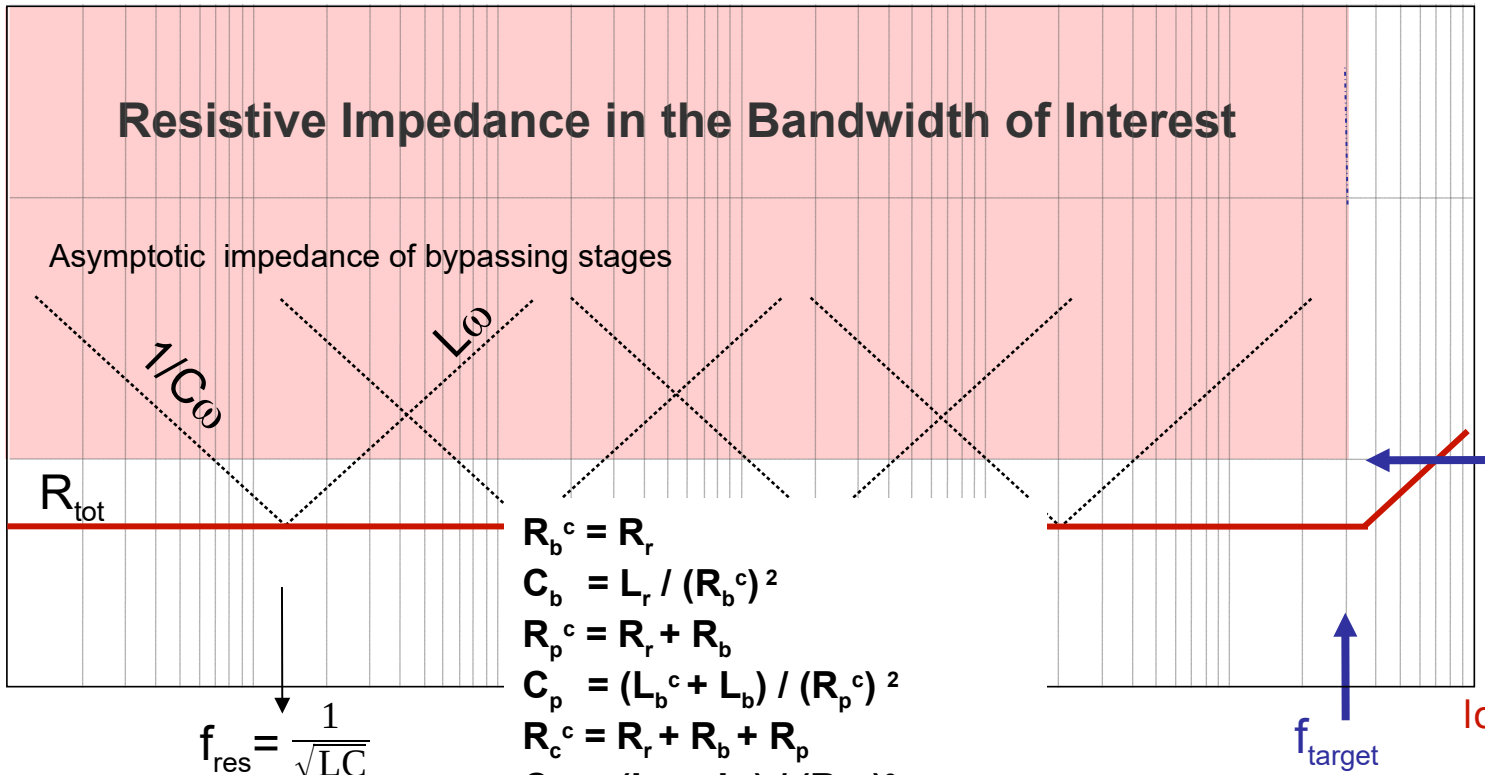
1- Bandwidth of Interest
2- Model of a Power Distribution System
3- Bypassing Examples
4- **Bypassing Methods**
5- IC and PCB Designers Point of View
6- Power Distribution System Model Extraction
7- Conclusion

Method to Flatten the Impedance of a PDS with HBC

A **full impedance compensation** at each bypassing stage



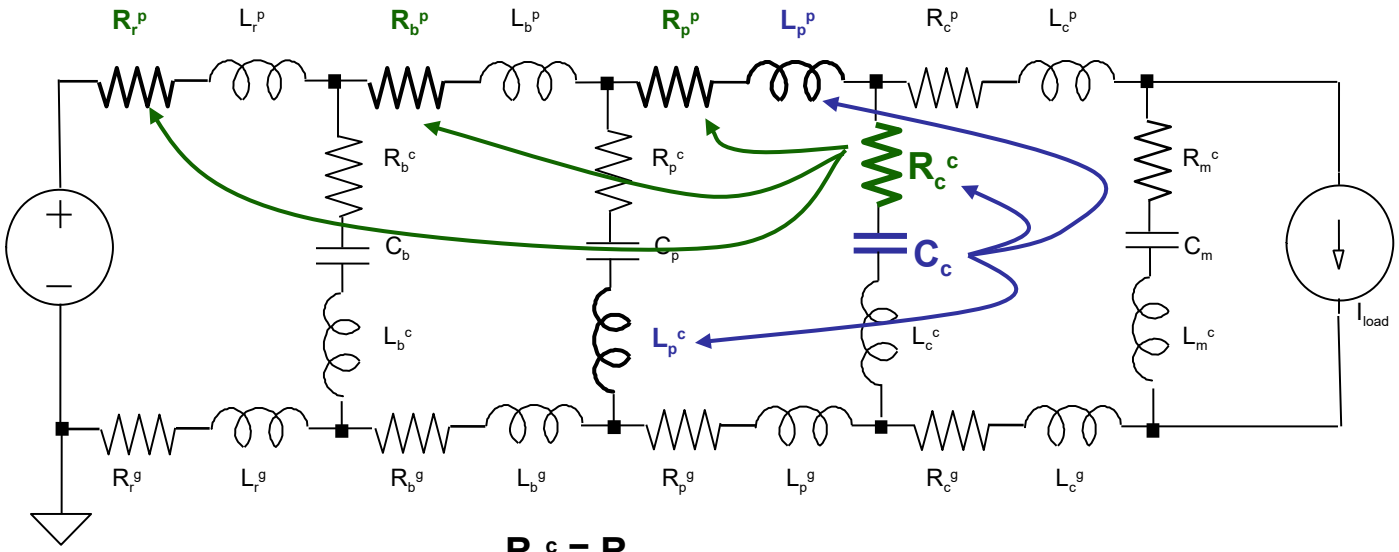
Z_{out} Magnitude, log|Ω|



$R_b^c = R_r$
$C_b = L_r / (R_b^c)^2$
$R_p^c = R_r + R_b$
$C_p = (L_b^c + L_b) / (R_p^c)^2$
$R_c^c = R_r + R_b + R_p$
$C_c = (L_p^c + L_p) / (R_c^c)^2$
$R_m^c = R_r + R_b + R_p + R_c = R_{tot}$
$C_m = (L_c^c + L_c) / (R_m^c)^2$

Method to Flatten the Impedance of a PDS with HBC

A full impedance compensation
at each bypassing stage



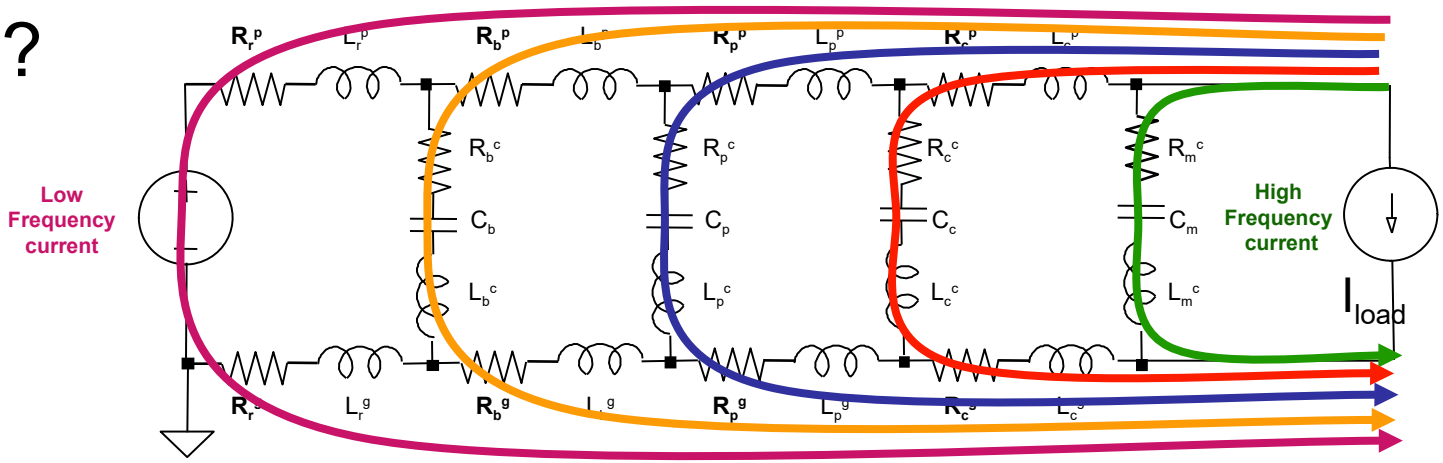
$$R_b^c = R_r$$
$$C_b = L_r / (R_b^c)^2$$

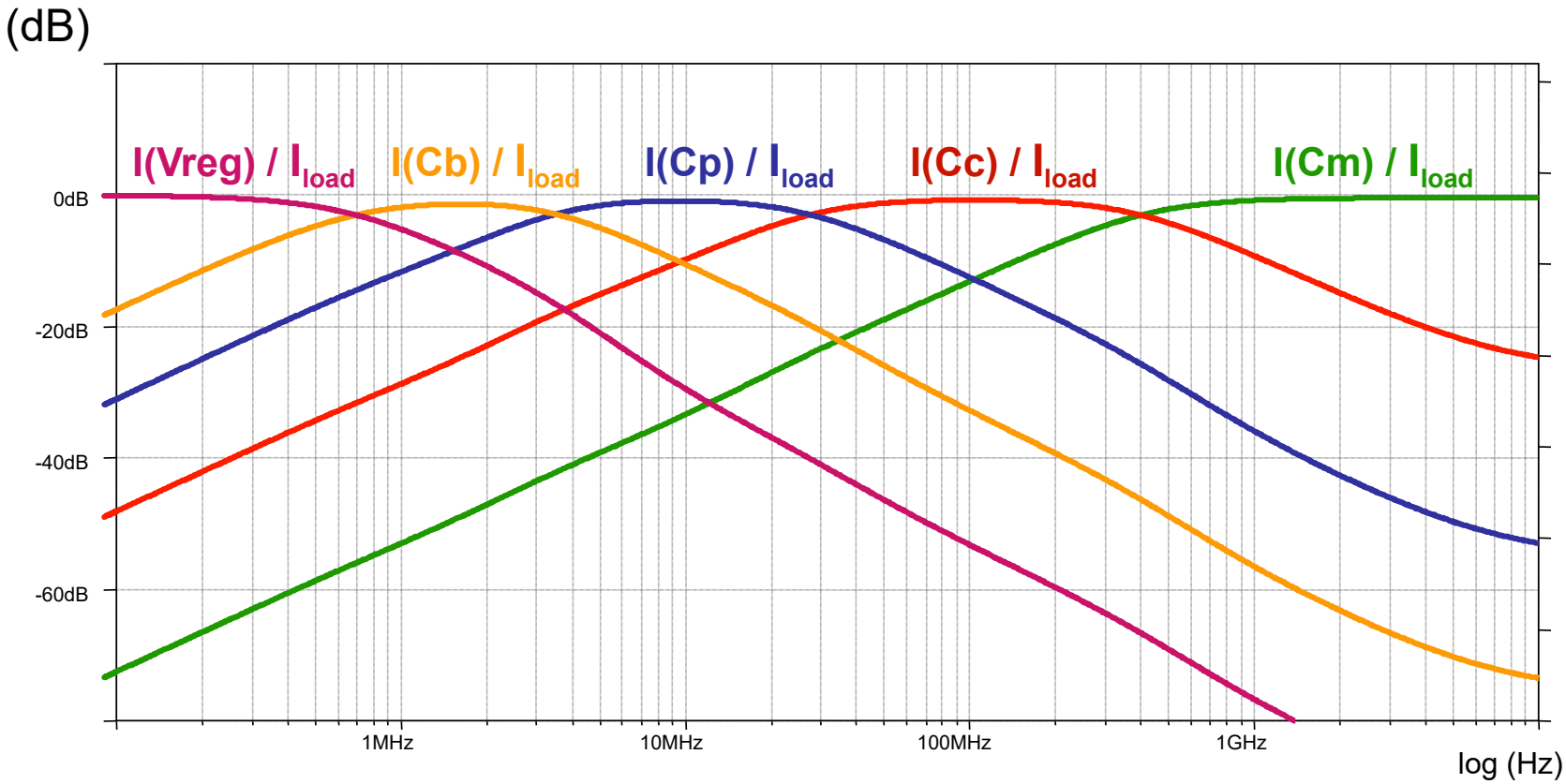
$$R_p^c = R_r + R_b$$
$$C_p = (L_b^c + L_b) / (R_p^c)^2$$

$$R_c^c = R_r + R_b + R_p$$
$$C_c = (L_p^c + L_p) / (R_c^c)^2$$

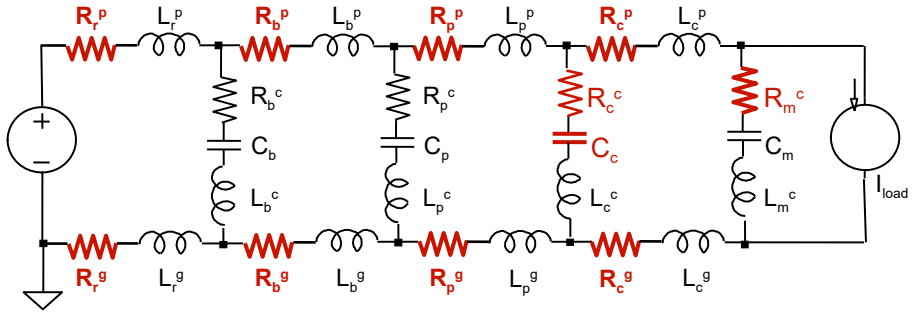
$$R_m^c = R_r + R_b + R_p + R_c = R_{tot}$$
$$C_m = (L_c^c + L_c) / (R_m^c)^2$$

How it Works?


Low Frequency current
High Frequency current
I_{load}
R_r^p
L_r^p
R_b^p
L_b^p
R_p^p
L_p^p
R_c^p
L_c^p
R_b^c
C_b
L_b^c
R_p^c
C_p
L_p^c
R_c^c
C_c
L_c^c
R_m^c
C_m
L_m^c
L_r^g
R_b^g
L_b^g
R_p^g
L_p^g
R_c^g
L_c^g


(dB)
I(Vreg) / I_{load}
I(Cb) / I_{load}
I(Cp) / I_{load}
I(Cc) / I_{load}
I(Cm) / I_{load}
0dB
-20dB
-40dB
-60dB
1MHz
10MHz
100MHz
1GHz
log (Hz)

Bypass Capacitors Computation




```
******  TARGET

.PARMS Z0 1.00
```

```
******  PDN BOARD

.PARMS Rr 0.25
.PARMS Lr 50.0nH

.PARMS Rb 0.10
.PARMS Lb 10.00nH
```

```
******  BYPASS ON THE BOARD

.PARMS RCb 0.25
.PARMS Cb  800.00nF
.PARMS   LCb 5.00nH

.PARMS RCp 0.35
.PARMS Cp  122.4nF
.PARMS   LCp 1.50nH
```

```
******  PDN IC

.PARMS Rp 0.05
.PARMS Lp 1.00nH

.PARMS Rc 0.10
.PARMS Lc 0.10nH
```

```
******  BYPASS ON THE IC

.PARMS RCc 0.4
.PARMS Cc  15.6nF
.PARMS   LCc 0.10nH

.PARMS RCm 0.5
.PARMS Cm  0.75nF
.PARMS   LCm 0.01nH
```

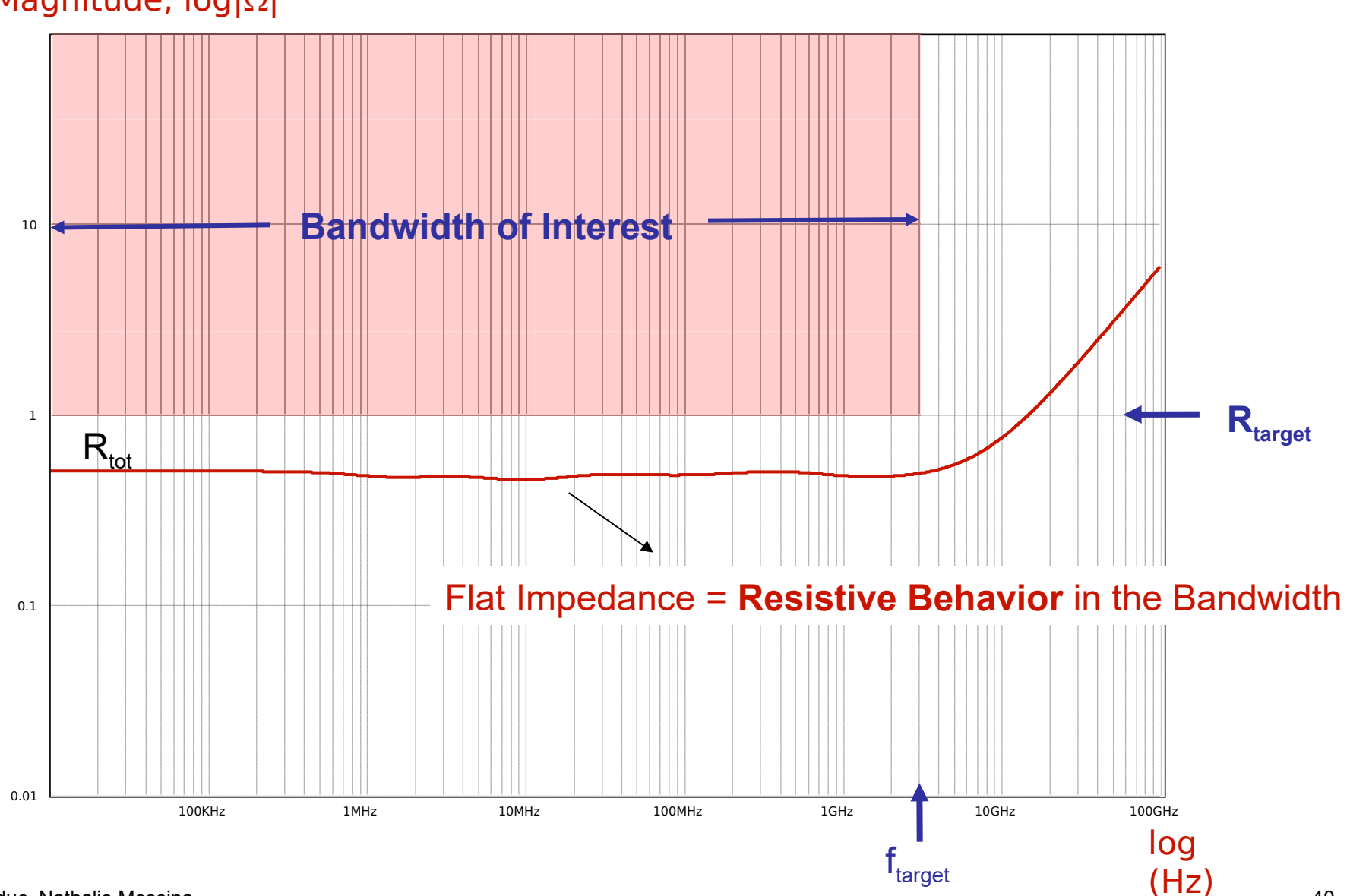
$R_b^c = R_r$
$C_b = L_r / (R_b^c)^2$

$R_p^c = R_r + R_b$
$C_p = (L_b^c + L_b) / (R_p^c)^2$

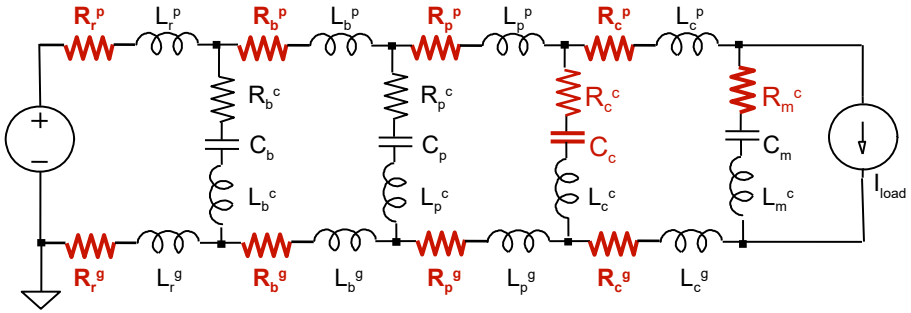
$R_c^c = R_r + R_b + R_p$
$C_c = (L_p^c + L_p) / (R_c^c)^2$

$R_m^c = R_r + R_b + R_p + R_c = R_{tot}$
$C_m = (L_c^c + L_c) / (R_m^c)^2$

Flat Impedance of a PDS with Hierarchical Bypass Caps



The ESR Issue




```
******  TARGET

.PARMS Z0 1.00
```

```
******  PDN BOARD

.PARMS Rr 0.25
.PARMS Lr 50.0nH

.PARMS Rb 0.10
.PARMS Lb 10.00nH
```

```
******  BYPASS ON THE BOARD

.PARMS RCb 0.25
.PARMS Cb  800.00nF
.PARMS   LCb 5.00nH

.PARMS RCp 0.35
.PARMS Cp  122.4nF
.PARMS   LCp 1.50nH
```

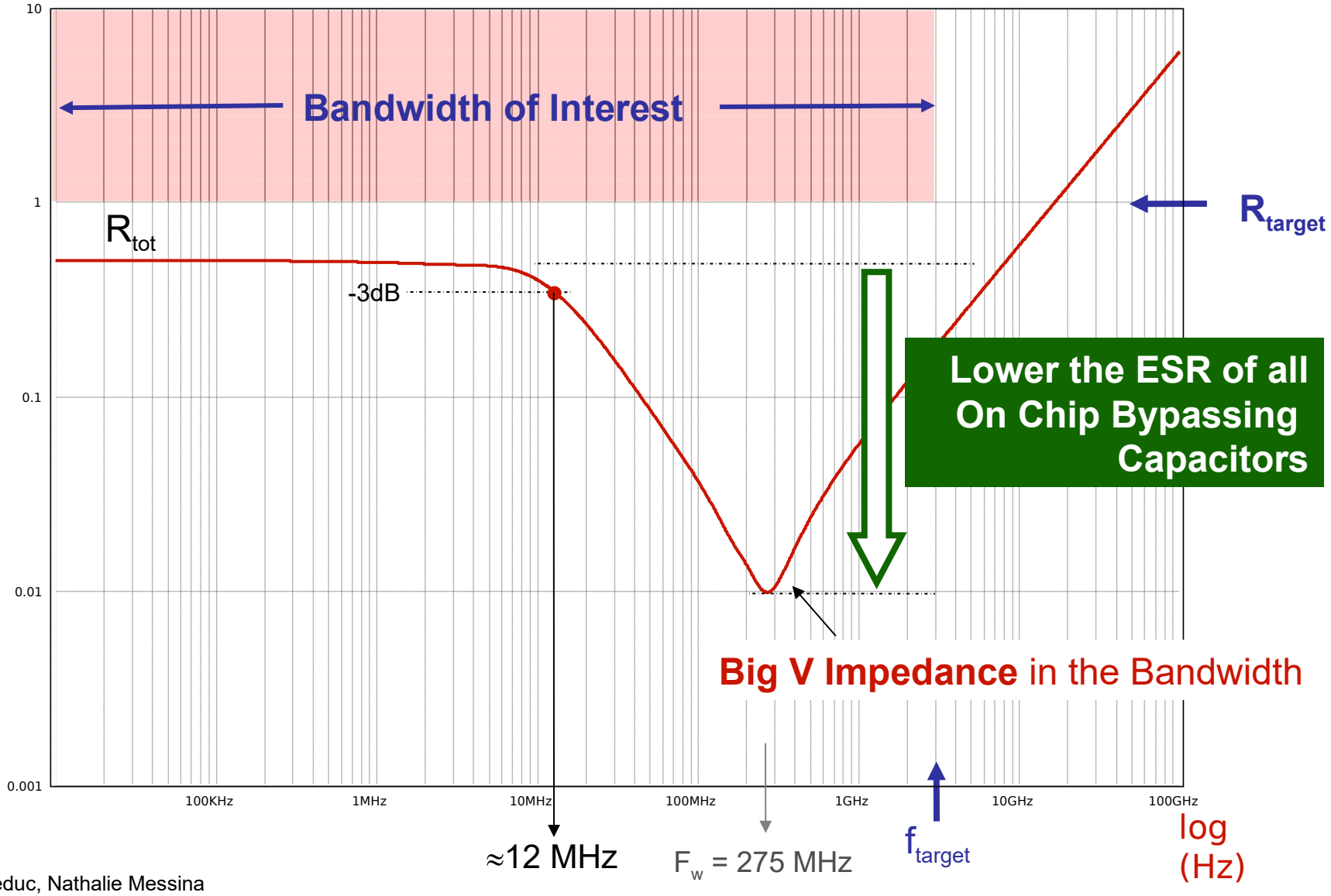
```
******  PDN IC

.PARMS Rp 0.05
.PARMS Lp 1.00nH

.PARMS Rc 0.10
.PARMS Lc 0.10nH
```

```
******  BYPASS ON THE IC

.PARMS RCc 0.4
.PARMS Cc  15.6nF
.PARMS   LCc 0.10nH

.PARMS RCm 0.5
.PARMS Cm  0.75nF
.PARMS   LCm 0.01nH
```

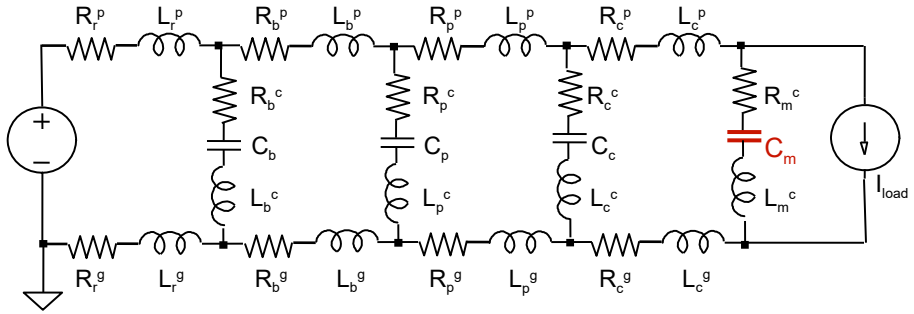
Impossible to realize such large ESR on Chip

Big V Impedance of a PDS

Z_{out} Magnitude, log|Ω|



The Big V Values



Values for a Flat Impedance

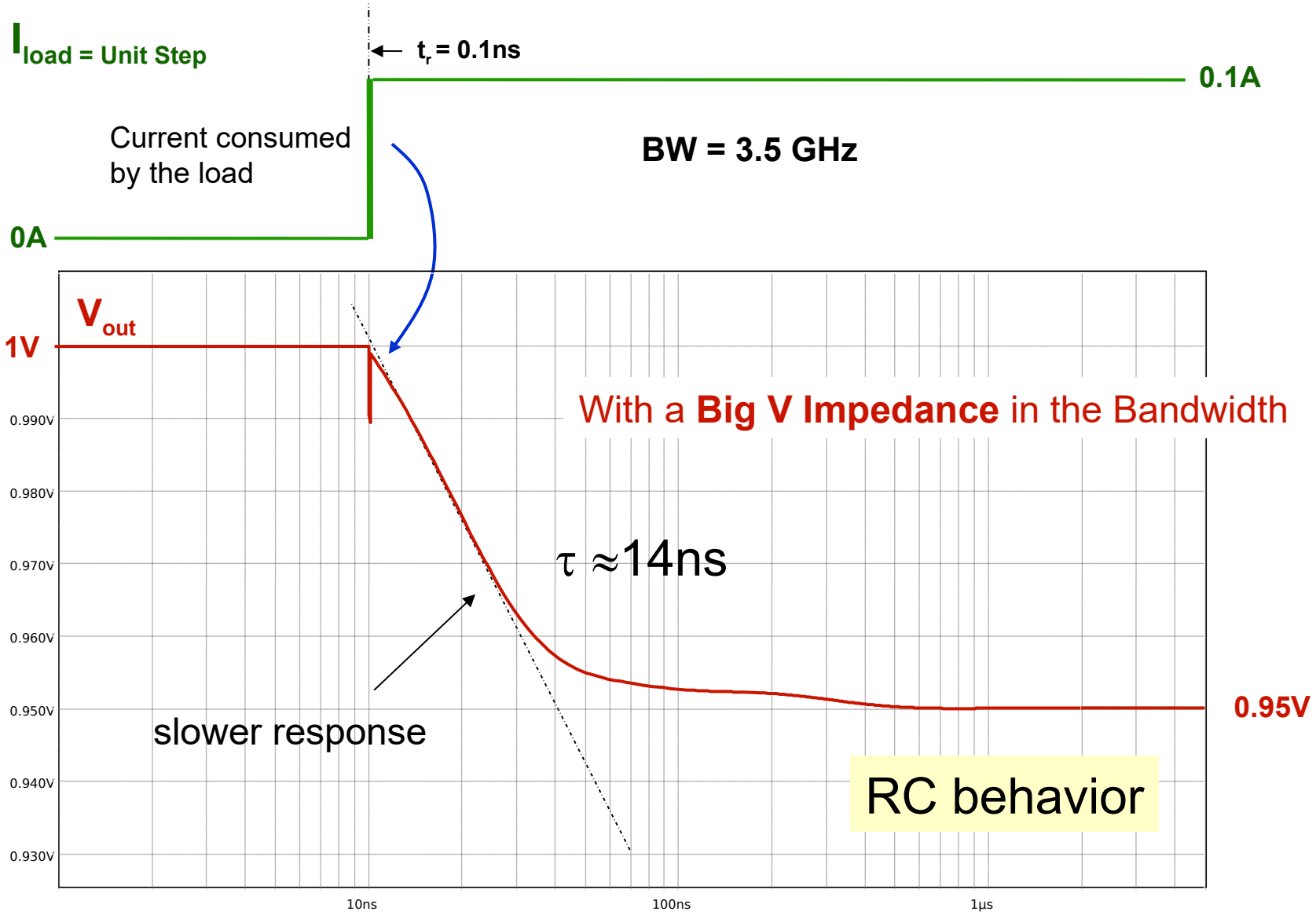
```
******  BYPASS ON THE BOARD

.PARMS RCb 0.25
.PARMS Cb  800.00nF
.PARMS   LCb 5.00nH

.PARMS RCp 0.35
.PARMS Cp  122.4nF
.PARMS   LCp 1.50nH

******  BYPASS ON THE IC

.PARMS RCc 0.4
.PARMS Cc  15.6nF
.PARMS   LCc 0.10nH

.PARMS RCm 0.5
.PARMS Cm  0.75nF
.PARMS   LCm 0.01nH
```

=

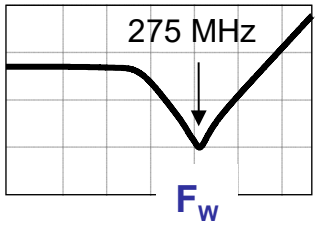
Values for a BigV Impedance

```
******  BYPASS ON THE BOARD

.PARMS RCb 0.25
.PARMS Cb  800.00nF
.PARMS   LCb 5.00nH

.PARMS RCp 0.35
.PARMS Cp  122.4nF
.PARMS   LCp 1.50nH

******  BYPASS ON THE IC

.PARMS RCc 0.01
.PARMS Cc  4.0nF
.PARMS   LCc 0.10nH

.PARMS RCm 0.01
.PARMS Cm 35.0nF
.PARMS   LCm 0.01nH
```

Transient on a PDS with Big V Impedance



Transient on a PDS around the Impedance Dip



Load Current @ 275 MHz

100mA
0mA

Full Impedance Compensation

Load

9 mV

0mV
-20mV
-40mV

-55 mV

If the operating frequency coincides to the frequency dip

Package

BigV

Big V is better!

0mV
-20mV

- 16 mV

- 34 mV

Load

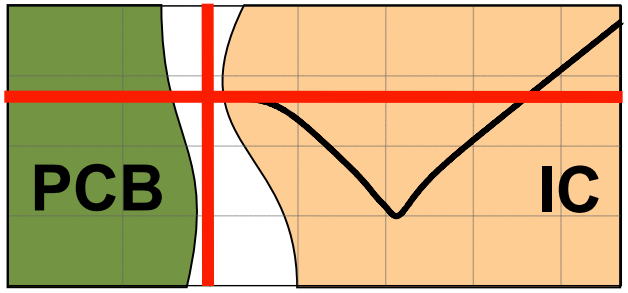
0ns
50ns
100ns

AGENDA

1- Bandwidth of Interest
2- Model of a Power Distribution System
3- Bypassing Examples
4- Bypassing Methods
5- **IC and PCB Designers Point of View**
6- Power Distribution System Model Extraction
7- Conclusion

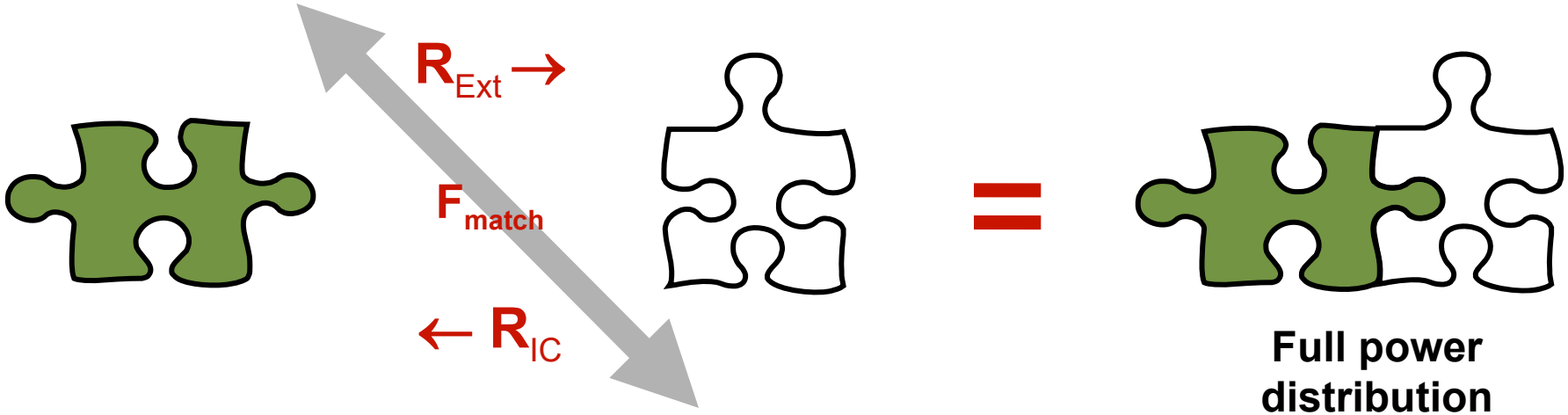
PCB Design, IC Design: Impedance Matching

$R_{tot} = R_{Ext} + R_{IC}$



F_{match}

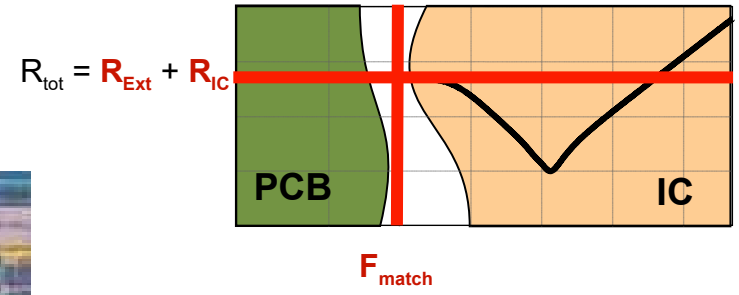
PCB bypassing, func(F_{match}, R_{IC} , R_{Ext})

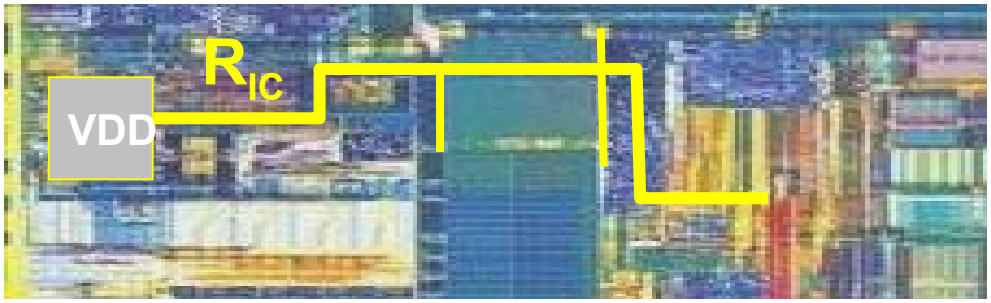


IC bypassing, func(F_{match}, R_{IC} , R_{Ext})

Full power distribution system bypassing

The IC Designer Point of View





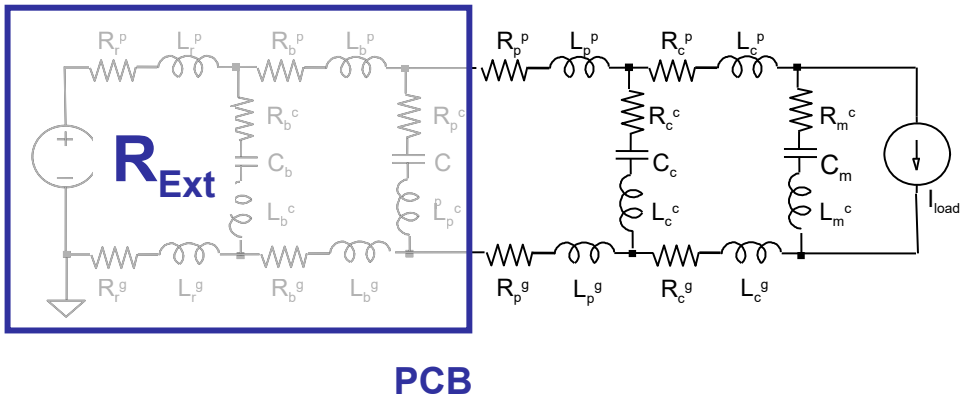
According to the design methodology presented in the previous slides,

the IC designer needs to fix the appropriate **Resistance Budget R_{Ext}** of the external power supply to obtain the specified performances.

The designer will use the **BigV method** to choose the bypass capacitors on the IC.

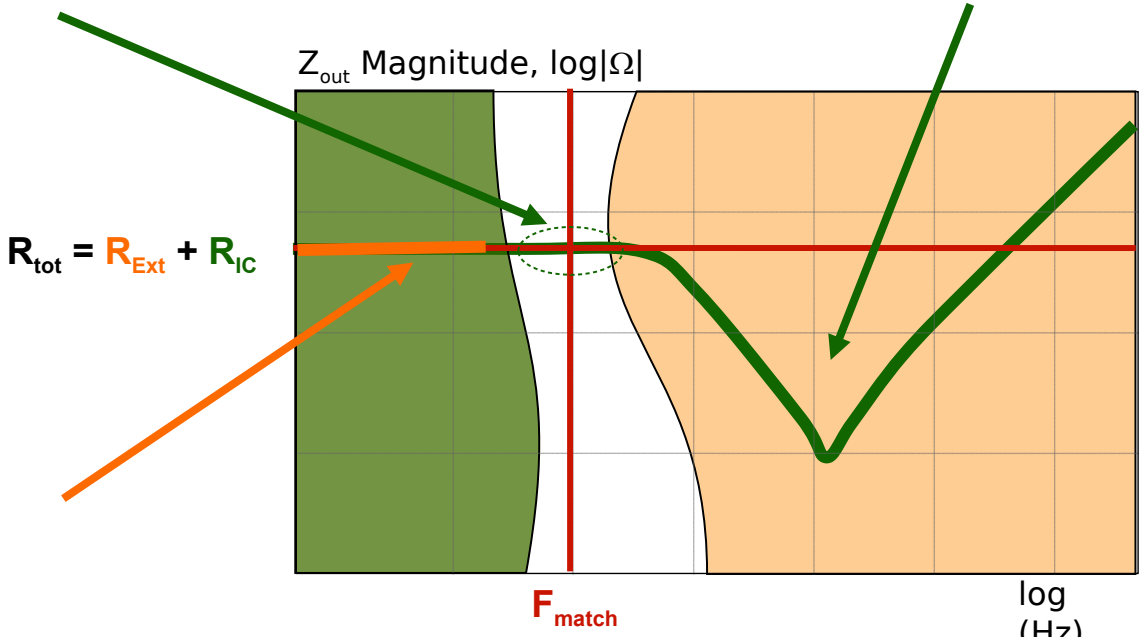
The IC designer will communicate to the PCB designer the resistance budget **R_{Ext}**, the internal resistance of the IC **R_{IC}** and the frequency **F_{match}**.

The Job of the IC Designer



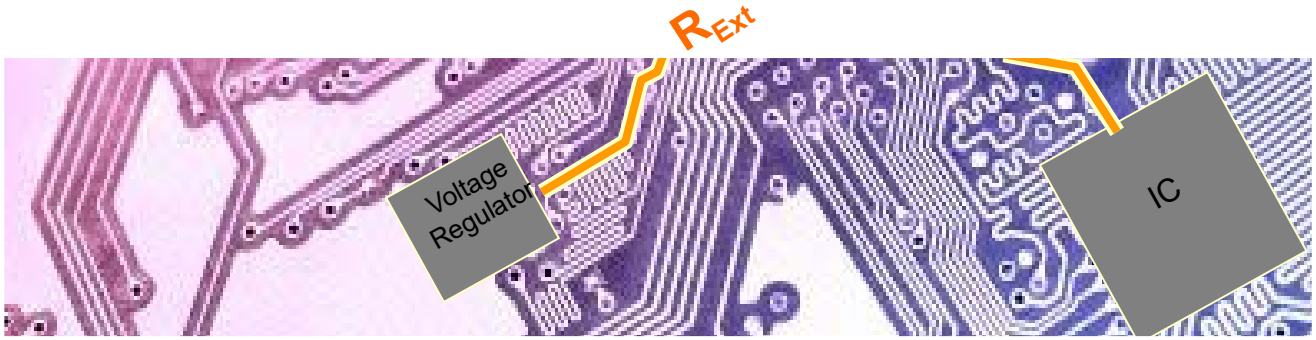
The IC must behave as a resistance R_{IC} at F_{match}

BigV bypassing method is recommended for frequencies above F_{match}



The PCB is modeled as a resistance R_{Ext}

The PCB Designer Point of View



According to the design methodology presented in the previous slides,

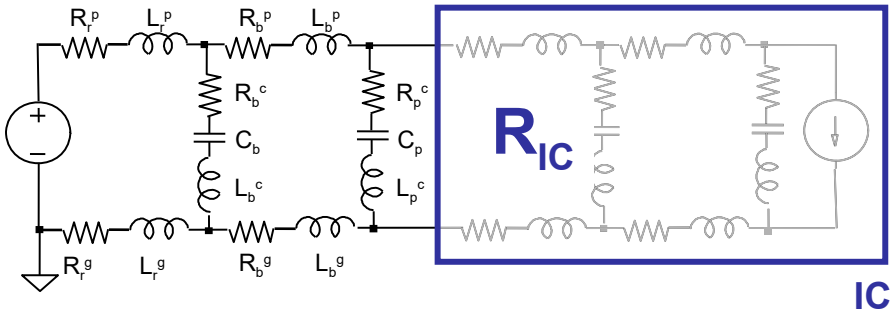
the PCB designer needs to know the **Resistance Budget R_{Ext}** of the power supply, the **Resistance of the IC R_{IC}** and the **Frequency F_{match}** to realize the impedance matching.

These resistances are provided by the IC vendor. R_{Ext} includes the PCB line resistance and the internal resistance of the voltage regulator.

$$R_{Ext} = R_{Regulator} + R_{PCB\ line}$$

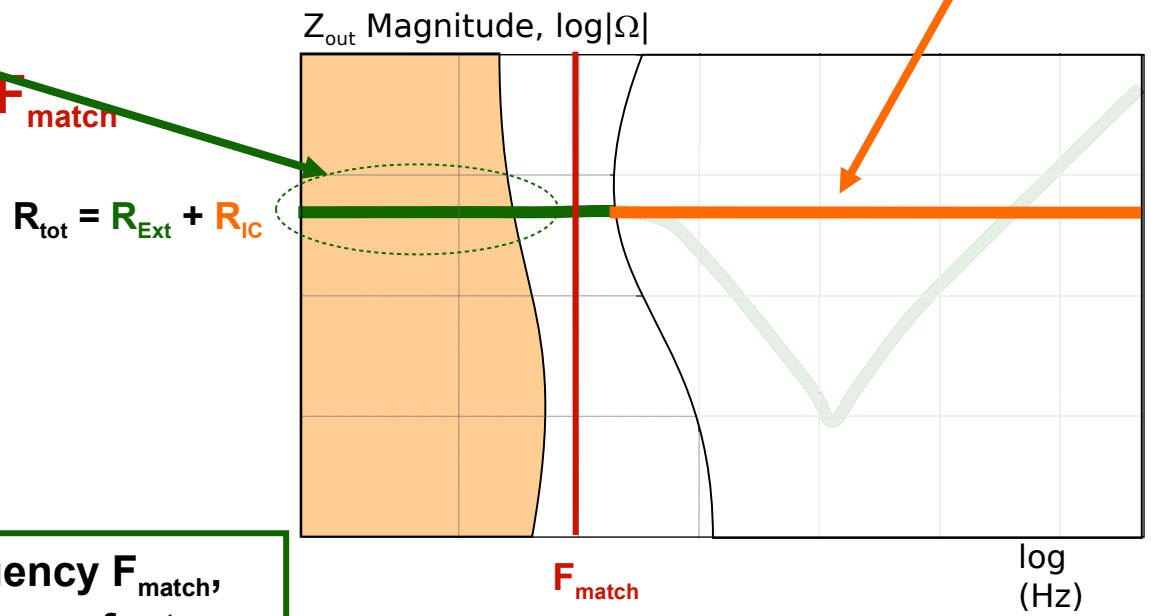
The PCB designer will then use the **Full Impedance Compensation method** to choose the bypass capacitors on the PCB.

The PCB Designer Point of View



The PCB must behave as a resistance R_{ext} below F_{match}

The IC is modeled as a resistance R_{IC}

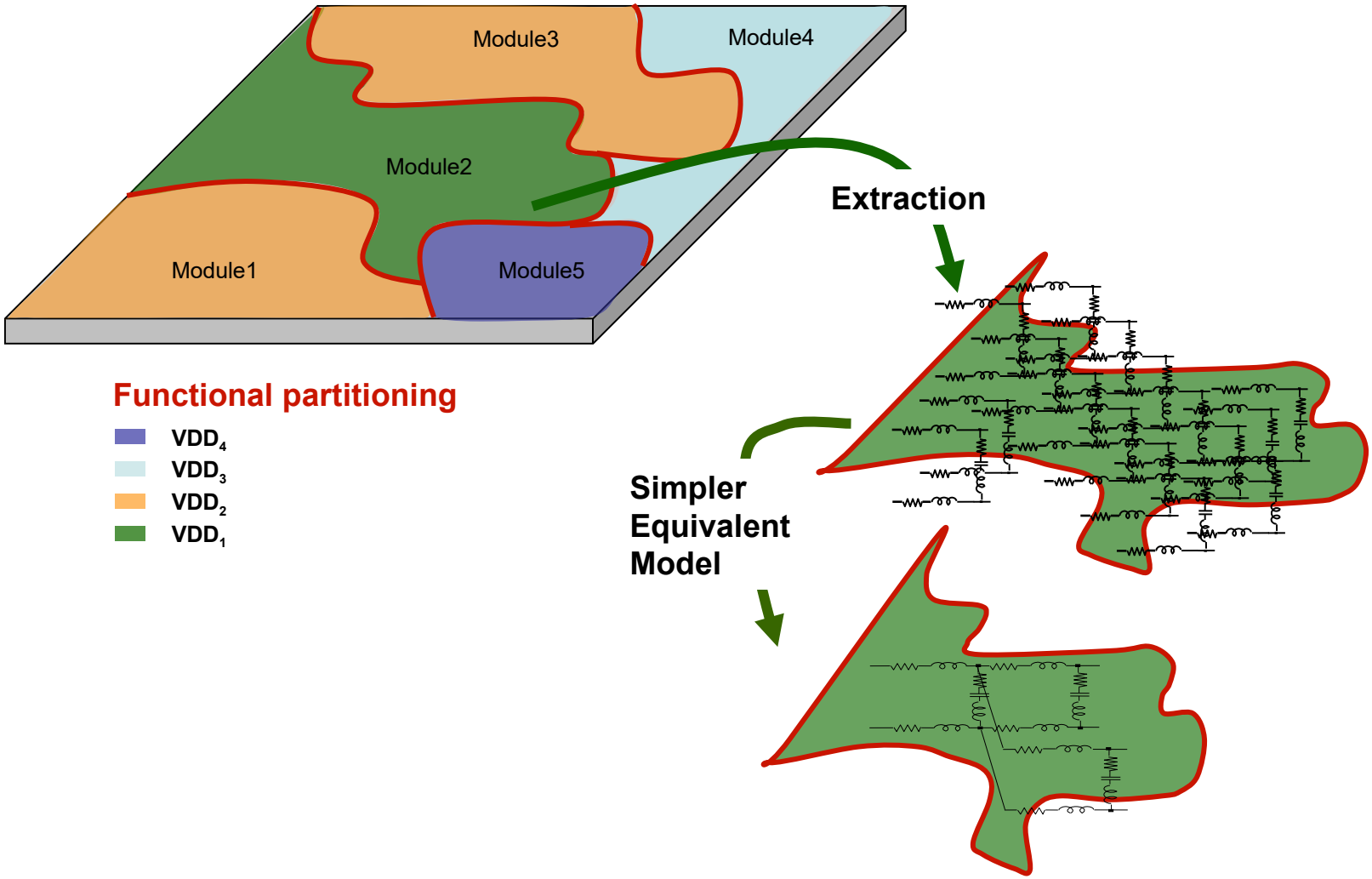


Using the R_{Ext}, R_{IC} and the Frequency F_{match}, the PCB designer is able to get a perfect impedance matching.

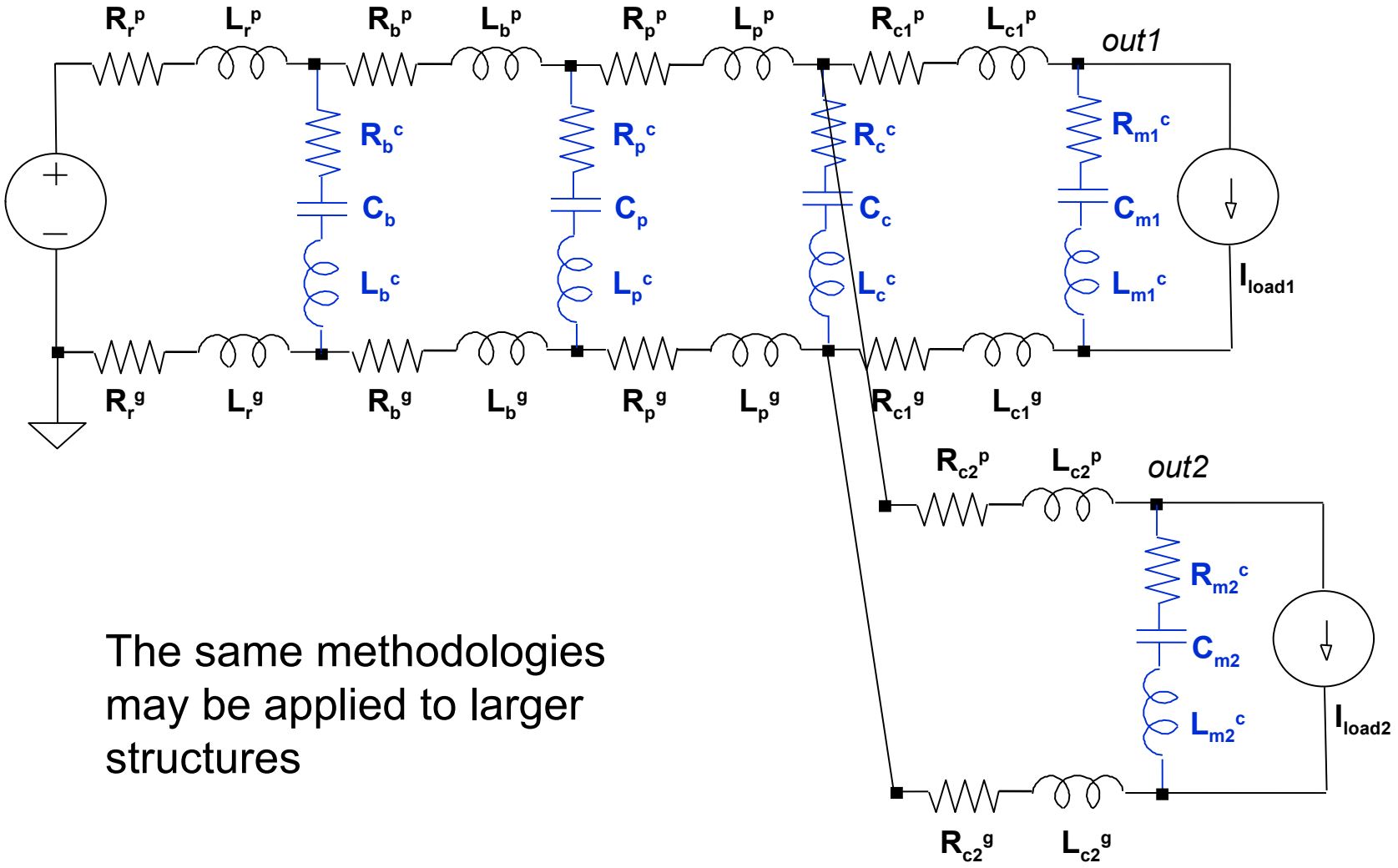
AGENDA

1- Bandwidth of Interest
2- Model of a Power Distribution System
3- Bypassing Examples
4- Bypassing Methods
5- IC and PCB Designers Point of View
6- **Power Distribution System Model Extraction**
7- Conclusion

Model Partitioning of a Power Distribution System



Model of a Power Distribution System with n Modules

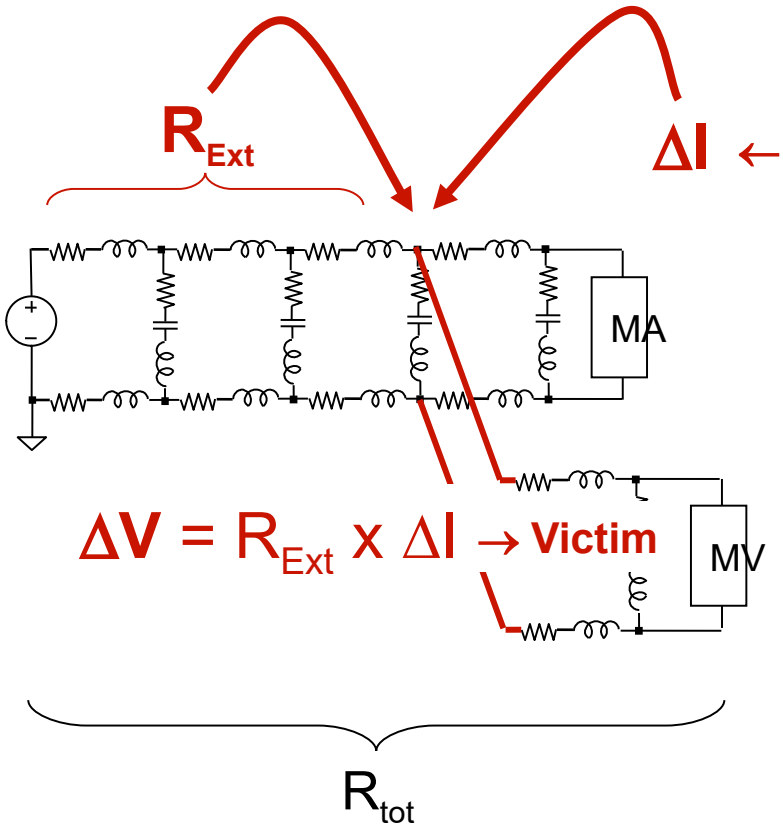


The same methodologies may be applied to larger structures

AGENDA

1- Bandwidth of Interest
2- Model of a Power Distribution System
3- Bypassing Examples
4- Bypassing Methods
5- IC and PCB Designers Point of View
6- Power Distribution System Model Extraction
7- **Conclusion**

Conclusion: Bypassing and Decoupling are **Essential**



$R_{tot} = R_{Ext} + R_{IC}$

A good bypassing does improve the decoupling.

Lowering R_{Ext} improves the decoupling of the system.

Best decoupling is obtained with low R_{Ext}.

Bypassing constrains R_{tot} R_{tot} *small*

Decoupling constrains R_{Ext} R_{Ext} *small*

A Few References

[PDN_04] Power Distribution Networks in High Speed Integrated Circuits
Andrey V. Mezhiba, Eby G. Friedman, 2004 by Kluwer Academic Publishers

[Fujitsu_02] Yoshihiko Imanaka, Takeshi Shioga, John D. Baniecki,
Decoupling Capacitor with Low Inductance for High Frequency Digital Applications
Fujitsu Sci. Tech. J., 38,1,p22-30 June 2002

[Free_06] Microprocessor Design Forum ISSCC 2006, Multi-Core Architectures, Designs and Implementation Challenges
Presentation of D. Bouvier, Freescale, challenge of High Performance Multi-Core Processors for embedded Infrastructure

[SPI_05] CEI-Europe Course on Signal and Power Integrity of High Speed System Design
Dr Istvan Novak, November 2005